

SoMs Power Architecture

miriac® MPX2020

System on Module based on NXP® QorIQ® P2020
CPU



Highlights

- up to 2 GB DDR2 memory, soldered, optional: with EEC
- up to four SerDes up to 3.125 GHz multiplexed across controllers
- two 208 Pin Zero Force Connectors, that make all I/O and bus signals available to the carrier board
- High precision RTC
- Scaling from a single core at 533 MHz (P1011) to a dual core at 1.2 GHz (P2020)





Product Description

The miriac® MPX2020 CPU Module is the first of a series of QorIQ® based products. The P2020 combines dual Power Architecture® e500v2 processor cores with system logic required for networking, wireless infrastructure and telecommunications applications.



Features

CPU	
Architecture:	PowerPC
Memory	
Flash:	up to 512 MB NAND Flash
Flash Card:	1x SD
High Speed IO	
SerDes lanes:	up to four SerDes up to 3.125 GHz multiplexed across controllers, e.g. - 3x PCI Express® - 2x SRIO or - 2x SGMII
USB 2.0:	1x USB 2.0
Operating Condition	
Temperature:	optional: ext. temp.
Mechanical	
Formfactor:	MPX-1, 77 mm x 66 mm
Software / Additional	
Software Support:	Linux Microware OS-9 VxWorks MicroC/OS-II QNX others are available on request

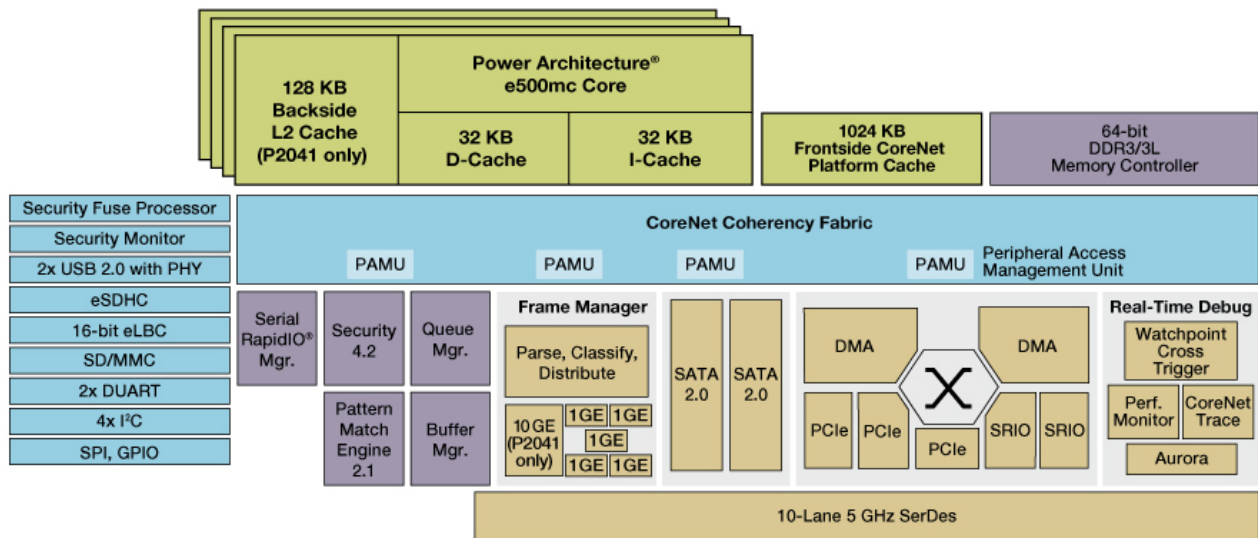
General Note:

Our standard product versions offer what we consider to be the optimum configuration in terms of performance, price, usage and TDP. The product features lists specify the maximum range of functions per interface. However, not all interfaces or functions are always available in parallel. Flexible SERDES multiplexing is one of the reasons for this. In addition, we provide multiple memory expansion options and are also happy to accommodate specific customer wishes. So do not hesitate to [contact us](#) directly to discuss your desired configuration.



Block Diagrams

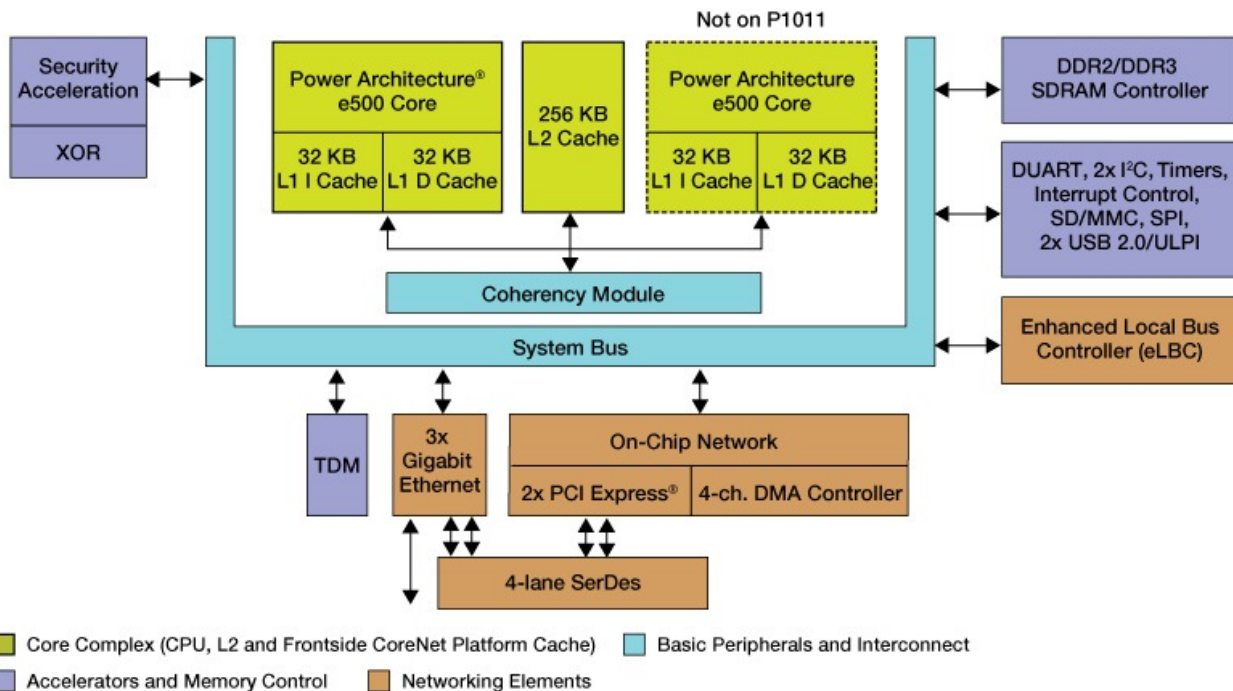
QorIQ P2040/P2041 Communication Processors



- Core Complex (CPU, L2 and Frontside CoreNet Platform Cache)
- Basic Peripherals and Interconnect
- Accelerators and Memory Control
- Networking Elements

NXP®_P2020_2010 Block Diagram

QorIQ P1020 and P1011 Block Diagram



- Core Complex (CPU, L2 and Frontside CoreNet Platform Cache)
- Basic Peripherals and Interconnect
- Accelerators and Memory Control
- Networking Elements

NXP®_P2020_2010 Block Diagram



Order Info

Name	Code	Description	Status
miriac® MPX2020	837612	2 QorIQ® e500v2, 1.2 GHz, 2 GB DDR2 w ECC, 4 MB NOR Flash, 256 MB NAND Flash, 0 °C to 70 °C, w/o SEC	EOL
	839610	miriac® SBC2020 development kit, incl. order #839601, Linux BSP, accessories	EOL
miriac® MPX2020	837605	2 QorIQ® e500v2, 1.0 GHz, 2 GB DDR2 w ECC, 4 MB NOR Flash, 256 MB NAND Flash, -40 °C to 85 °C, w/o SEC	EOL



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