

Microsys

User's Manual

SR001

5th edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
D-82054 Sauerlach
Germany

declare that the product

SR 001

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above-mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

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Edition

	Date:	Ident-Nr.:	Released:
Manual	23.04.03	EW204MA-01AC	
Default Jumper setting changed for 512K SRAMs. Drawings added on page 44 and 54. Hint for address decoding added on page 10.			
Schematics	27.09.88	SR 001 Rev.2	

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1. INTRODUCTION

1.1 Short Description

The **SR 001** is another product from the EuroONE-VMEbus-Line from MicroSys.

This static RAM/ROM-Board is divided into 3 banks, each having 4 JEDEC-Sockets, where either 28 or 32 pin Chips can be installed. Therefore SRAMs up to 128K x 8, EPROMs up to 1M x 8 as well as EEPROMS, ROMs etc. can be used. The access time and base address for each bank is jumper selectable.

Each bank can be write protected i.e. no write access can be performed on the bank. The write protect feature can be activated by using the switch on the front of the board.

The SR 001 also features Battery Backup for SRAMs, which allows for data retention during power failure or power-down. Either 3 NiCd-Accumulators or 1 Lithium-Battery can be used.

The highly integrated design of the SR 001, offers an outstanding price/performance ratio.

The Single Euro Format allows for:

- a better resistance against vibrations and shocks
- more compact system packaging.

1.2 Features

- Single Eurocard Format
- 12 JEDEC Sockets
- Board divided into 3 banks
- Selectable bank base address
- Each bank individually configured for size
- SRAMs, EPROMs, EEPROMS and ROMs can be used
- Bank Select LED
- Selectable Access Time for each bank
- Write protection from front panel
 - LED indicator
- Battery Backup for each bank
- 6 status LEDs
- VMEbus Slave
 - A24/D16/D8
- Selectable AM Codes

1.3 Options

- Front Panel

1.4 Specifications

— Power Requirements (typ)	5V +/- 5% 0.4A +12V +/- 10% 0.1mA -12V +/- 10% 0.1mA
— Environmental Requirements	
Operating Temperature	0 degrees C to + 45 degrees C (due to accumulator)
Relative Humidity	0 to 95% (non-condensing)
Storage Temperature	-15 degrees C to +85 degrees C
— Board Dimensions	Single Euro Format

2. DELIVERY

2.1 The following items are shipped with this unit

- User's Manual
- MicroSys shipping carton

ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys Shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

3. INSTALLATION

3.1 Items required for SR 001 installation

For the installation of the SR 001, the following items are required.

- Card Cage or housing
- VMEbus Motherboard
- Adequate rated power supply

3.2 Points to be observed with unit

Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +5V (+/-5%), +12V and -12V (+/-10%)
- Be sure voltage is of correct polarity
- Unit should only be inserted into, and removed from card cage when power is off
- The card cage should be well ventilated. The Operating temperature should never exceed its specified range
- Check default jumper settings, refer to page 44

**GUARANTEE IS VOID IF UNIT IS OPERATED
OUT OF IT'S SPECIFICATIONS!**

With the above points adhered to, the unit can be inserted into the card cage.

4. Board Description

Table 1: RAM/ROM Chip-Decoding SR 001 :

Type	Decoding Size (Hex)	Comment
SRAM Bank A	00 7FFF	Chip-Size 8K x 8
SRAM Bank A	00 FFFF	Chip-Size 16K x 8
SRAM Bank A	01 FFFF	Chip-Size 32K x 8
SRAM Bank A	03 FFFF	Chip-Size 64K x 8
SRAM Bank A	07 FFFF	Chip-Size 128K x 8
SRAM Bank A	0F FFFF	Chip-Size 256K x 8
SRAM Bank A	1F FFFF	Chip-Size 512K x 8
SRAM Bank A	3F FFFF	Chip-Size 1024K x 8
SRAM Bank B	00 7FFF	Chip-Size 8K x 8
SRAM Bank B	00 FFFF	Chip-Size 16K x 8
SRAM Bank B	01 FFFF	Chip-Size 32K x 8
SRAM Bank B	03 FFFF	Chip-Size 64K x 8
SRAM Bank B	07 FFFF	Chip-Size 128K x 8
SRAM Bank B	0F FFFF	Chip-Size 256K x 8
SRAM Bank B	1F FFFF	Chip-Size 512K x 8
SRAM Bank B	3F FFFF	Chip-Size 1024K x 8
SRAM Bank C	00 7FFF	Chip-Size 8K x 8
SRAM Bank C	00 FFFF	Chip-Size 16K x 8
SRAM Bank C	01 FFFF	Chip-Size 32K x 8
SRAM Bank C	03 FFFF	Chip-Size 64K x 8
SRAM Bank C	07 FFFF	Chip-Size 128K x 8
SRAM Bank C	0F FFFF	Chip-Size 256K x 8
SRAM Bank C	1F FFFF	Chip-Size 512K x 8
SRAM Bank C	3F FFFF	Chip-Size 1024K x 8

4.1 RAM/ROM Sockets

The SR 001 has twelve 32 pin Sockets onboard, which are divided into three banks of four Sockets. Each bank represents a RAM- or ROM-Area, which is completely independent from the other two. Either 32 pin or 28 pin chips can be inserted into the sockets. The chip size can vary from bank to bank, but must not be different within a bank. All SRAMs, PROMs, EPROMS or EEPROMS of various sizes and access speeds, which meet the JEDEC pin standard can be inserted on the board.

Each bank has the following features:

- Selectable base address
- Eight various decoding sizes
- Four different access speeds
- Selectable AM-Codes: supervisor or user-access
- Write protection switch with LED indicator
- Battery backup
- Bank select LED



Note!

The memory banks cannot be disabled.

If e.g. only one bank is used, the other banks may be set to the same base address.

Decoding of bank B overrides bank A, bank C overrides bank A and B.

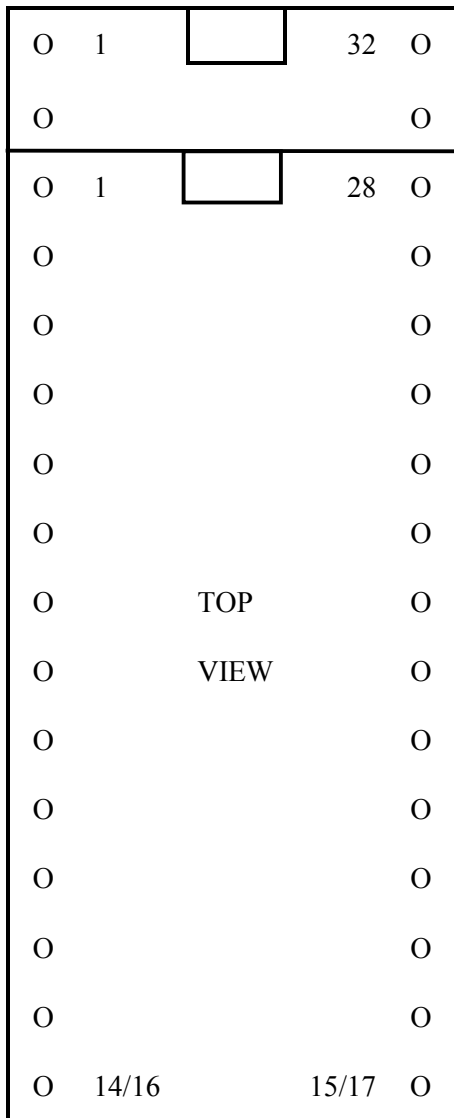
This means, if the address ranges overlap, bank C has the highest and bank A the lowest priority. Therefore bank C should be used first if not all memory sockets are populated.

In overlapping address ranges the bank select LEDs of all decoded banks are activated.

Socket Description for RAM/ROM Sockets J4-J7 and J11-J18:

32 pin and 28 pin chips must be inserted as shown below!

Any other insertion can destroy the chip and/or the board!



4.1.1 RAM/ROM Bank A

The 32 pin sockets J4 to J6 represent Bank A, while J4 and J6 refer to the lower half and J5 and J7 to the upper half Bank. The chips J4 and J5 contain the Most Significant Byte, J6 and J7 the Least Significant Byte of these two half banks. The pin configuration for different chip types is done using jumper field AA, which is located underneath the socket of J15.

With the jumper ABC, four different access times can be chosen which are further explained.

The base address selection for Bank A is made by the jumpers AC and AD. Jumper AC has got three selectable positions, 1-2, 2-3 and 4-5 for the decoding of VME-A15.

Position 3-4 performs the same selection as position 2-3. More than one of the four possible settings done at a time may cause permanent damage to the board!

With jumper field AD, the VME-Address-Lines A16 to A23 are decoded. These eight jumpers can be set to low or high decoding or ignoring the specified address line, depending on the used chip size and base address.

Depending on the memory size of the used chips, jumper AF must be set to the proper value. Because only one specific chip type must be inserted in a RAM/ROM Bank at a time, only one jumper must be set. More than one setting at a time will cause permanent damage to the board!

If 8Kx8 RAM-Chips are used, which got an additional high active chip select, jumper AB must be dropped to set pin 28 of the 32 pin sockets of Bank A to a high level. If this jumper is installed the described pin is connected to the address line A14.

When battery backup is needed, jumper AE must be set to position 2-3. For standard non-battery backup mode this jumper must be set to position 1-2.

The front panel switch SW1 enables the write protect function of Bank A when Led 2 is illuminated. Led 1 indicates any read or write access to Bank A.

The different AM Codes for Bank A can be set by jumper DA 1-2 and DA 3-4.

4.1.2 RAM/ROM Bank B

The 32 pin sockets J15 to J18 represent Bank B, while J16 and J18 refer to the lower half and J15 and J17 to the upper half Bank. The chips J15 and J16 contain the Most Significant Byte, J17 and J18 the Least Significant Byte of these two half banks. The pin configuration for different chip types is done using jumper field BA, which is located underneath the socket of J11.

With the jumper ABC, four different access times can be selected, which are described later.

The base address selection for Bank B is made by the jumpers BC and BD. Jumper BC has got three selectable positions, 1-2, 2-3 and 4-5 for the decoding of VME-A15.

Position 3-4 performs the same selection as position 2-3. More than one of the four possible settings done at a time may cause permanent damage to the board!

With jumper field BD, the VME-Address-Lines A16 to A23 are decoded. These eight jumpers can be set to low or high decoding or ignoring the specified address line, depending on the used chip size and base address.

Depending on the memory size of the used chips, jumper BF must be set to the proper value. Because only one specific chip type must be inserted in a RAM/ROM Bank at a time, only one jumper must be set. More than one setting at a time will cause permanent damage to the board!

If 8Kx8 RAM-Chips are used, which got an additional high active chip select, jumper BB must be dropped to set pin 28 of the 32 pin sockets of Bank B to a high level. If this jumper is installed the described pin is connected to the address line A14.

When battery backup is needed, jumper BE must be set to position 2-3. For standard non-battery backup mode this jumper must be set to position 1-2.

The front panel switch SW2 enables the write protect function of Bank B when Led 4 is illuminated. Led 3 indicates any read or write access to Bank B.

The different AM Codes for Bank B can be set by jumper DA 5-6 and DA 7-8.



Note!

If address ranges overlap, decoding of bank B overrides bank A.

4.1.3 RAM/ROM Bank C

The 32 pin sockets J11 to J14 represent Bank C, while J11 and J13 refer to the lower half and J2 and J14 to the upper half Bank. The chips J11 and J12 contain the Most Significant Byte, J13 and J14 the Least Significant Byte of these two half banks. The pin configuration for different chip types is done by jumper field CA, which is located underneath the socket of J15.

With the jumper ABC, four different access times are possible, like for Bank A and B.

The base address selection for Bank C is made by the jumpers CC and CD. Jumper CC got three selectable positions, 1-2, 2-3 and 4-5 for the decoding of VME-A15.

Position 3-4 performs the same selection as position 2-3. More than one of the four possible settings done at a time may cause permanent damage to the board!

With jumper field CD the VME-Address-Lines A16 to A23 are decoded. These eight jumpers can be set to low or high decoding or ignoring the specified address line, depending on the used chip size and base address.

Depending on the memory size of the used chips, jumper CF must be set to the proper value. Because only one specific chip type must be inserted in a RAM/ROM Bank at a time, only one jumper must be set. More than one setting at a time will cause permanent damage to the board!

If 8Kx8 RAM-Chips are used, which got an additional high active chip select, jumper CB must be dropped to set pin 28 of the 32 pin sockets of Bank C to a high level. If this jumper is installed the described pin is connected to the address line A14.

When battery backup is needed, jumper CE must be set to position 2-3. For standard non-battery backup mode this jumper must be set to position 1-2.

The front panel switch SW3 enables the write protect function of Bank C when Led 6 is illuminated. Led 5 indicates any read or write access to Bank C.

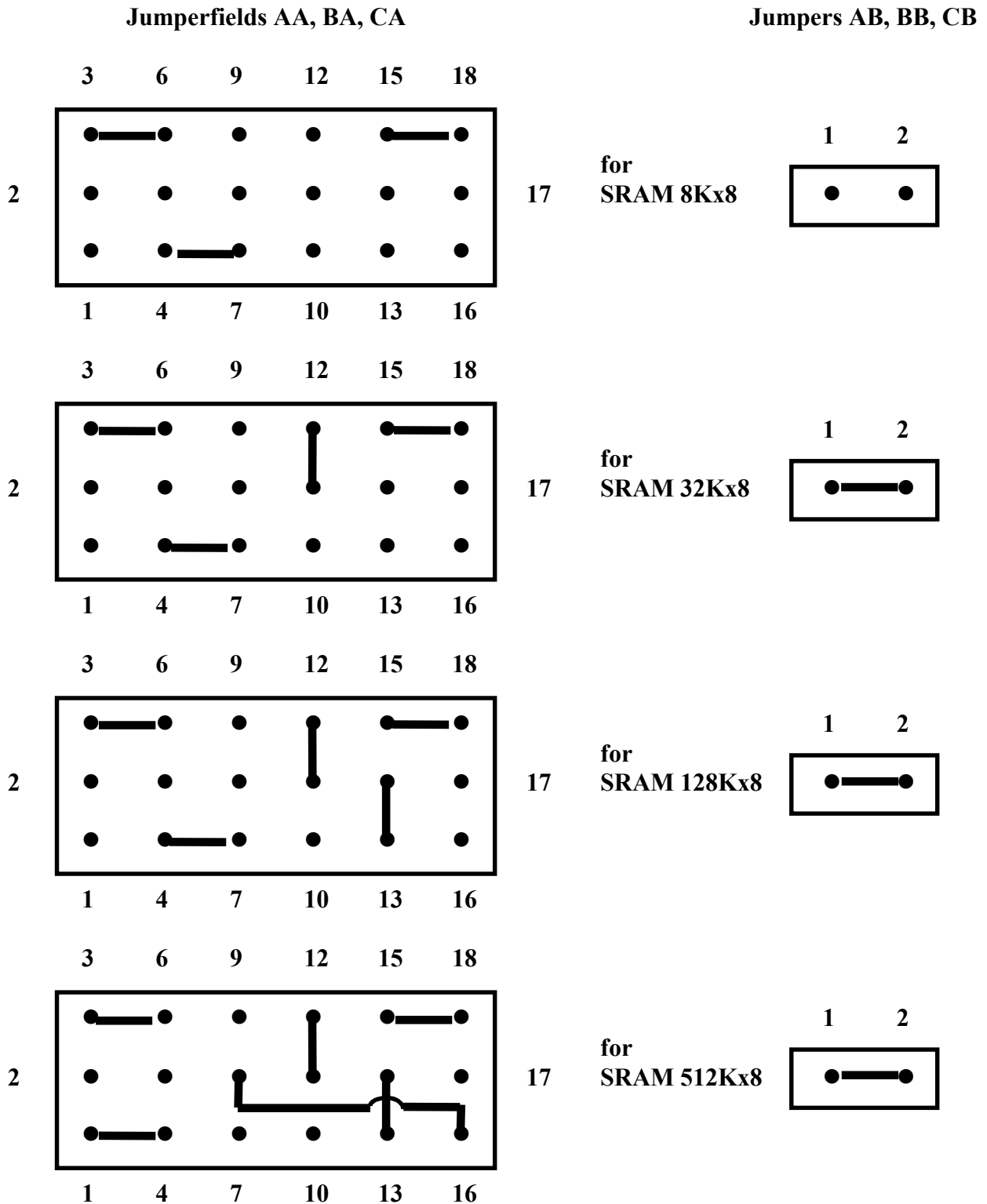
The different AM Codes for Bank C can be set by jumper DA 9-10 and DA 11-12.



Note!

If address ranges overlap, decoding of bank C overrides bank A and B.

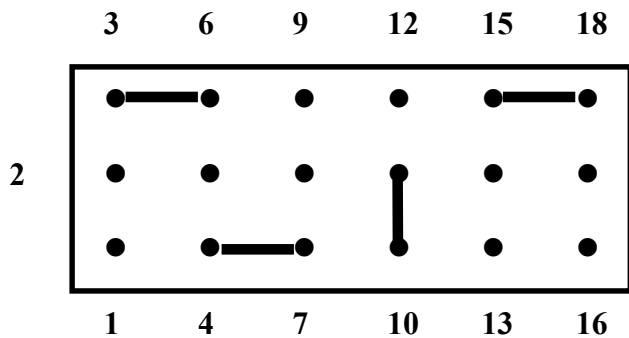
4.2 Setting of Memory Type



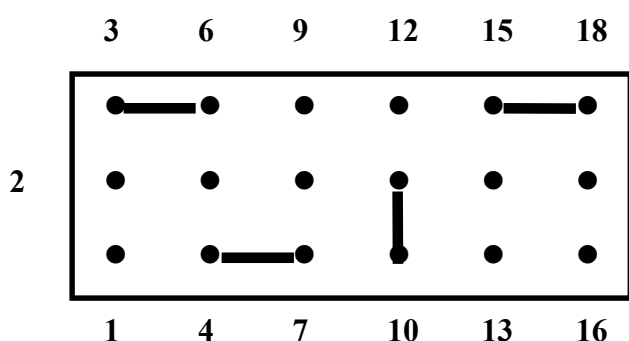
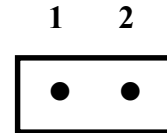
Attention! These jumpers are CHIP-Dependant!
Any jumper settings not in accordance with the chip specifications may cause permanent damage to either the board and/or the chips!

Jumper fields AA, BA, CA

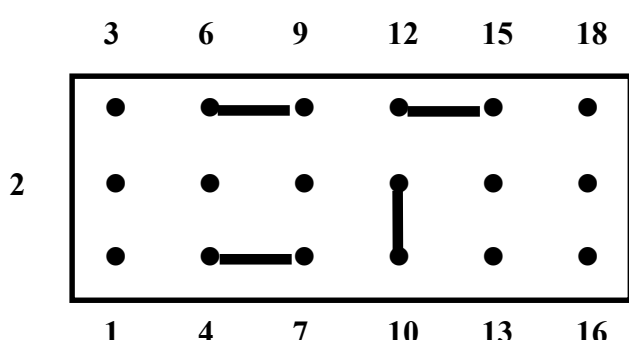
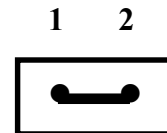
Jumpers AB, BB, CB



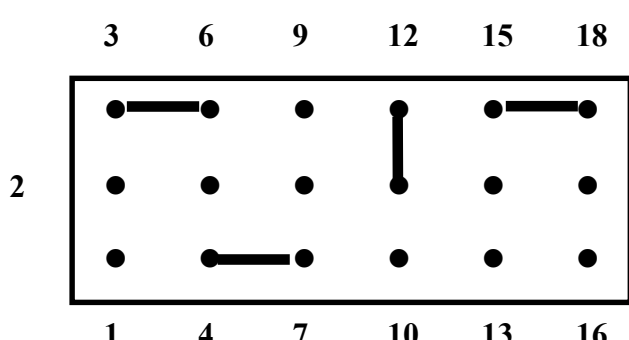
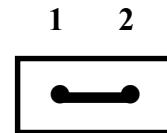
17 for EPROM 8Kx8 (2764)



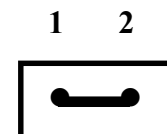
17 for EPROM 16Kx8 (27128)



17 for EPROM 32Kx8 (27256)



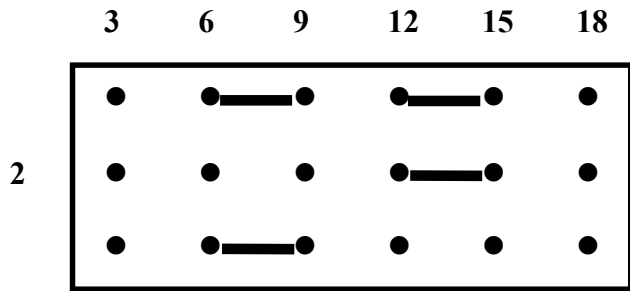
17 for EEPROM 32Kx8 (28256)



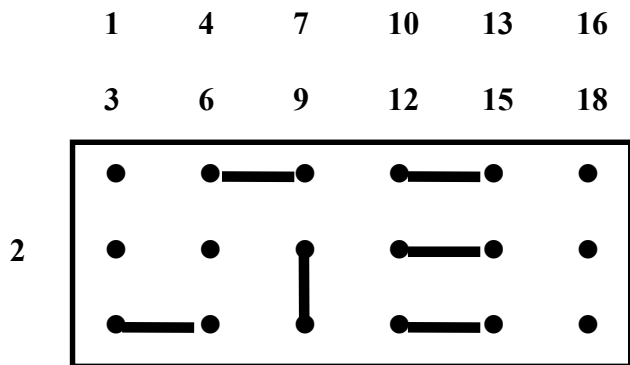
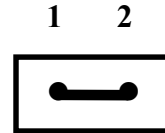
Attention! These jumpers are CHIP-Dependant!
Any jumper settings not in accordance with the chip specifications may cause permanent damage to either the board and/or the chips!

Jumper fields AA, BA, CA

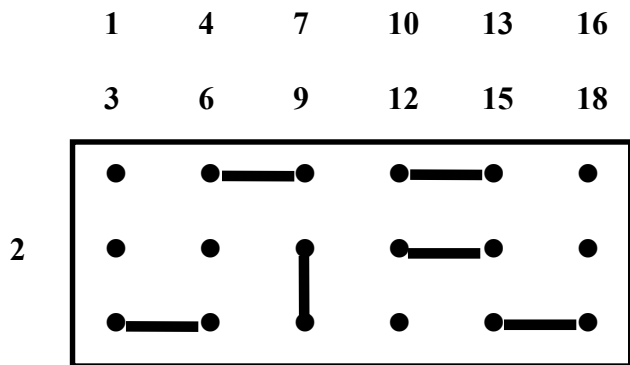
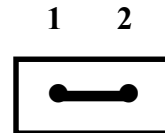
Jumpers AB, BB, CB



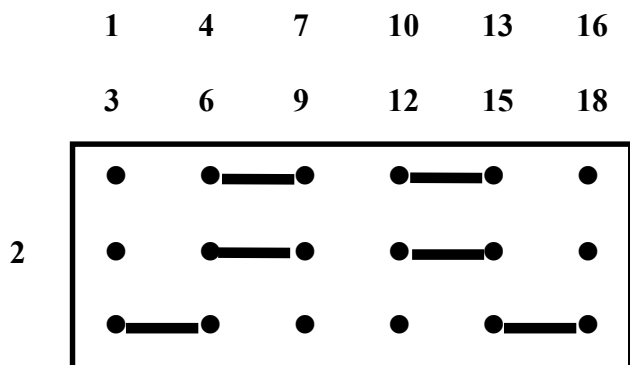
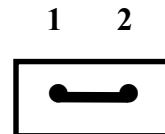
17 for
EPROM 64Kx8
(27512)



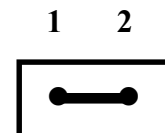
17 for
EPROM 128Kx8
EPROM 256Kx8
(27C1001 /
27C2001)



17 for
EPROM 512Kx8
(27C4001)



17 for
EPROM 1MBx8
(27C8001)



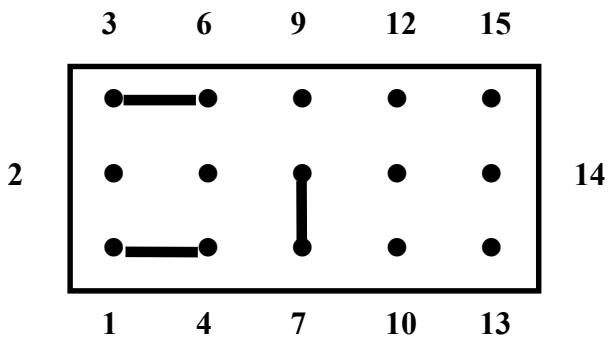
Attention! These jumpers are CHIP-Dependant!
Any jumper settings not in accordance with the chip specifications may cause permanent damage to either the board and/or the chips!

4.3 Setting of Chip Access Time of Banks A, B & C

Possible Access-Times: 100ns 150ns 200ns 250ns

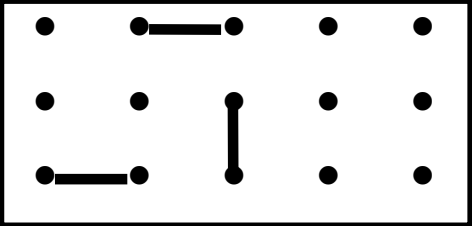
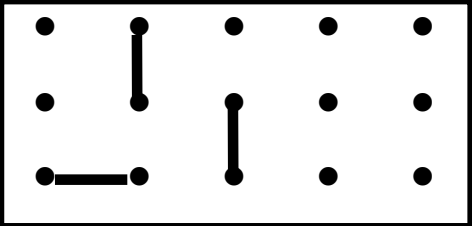
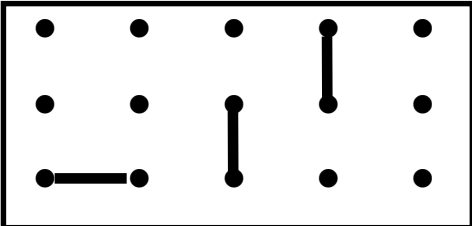
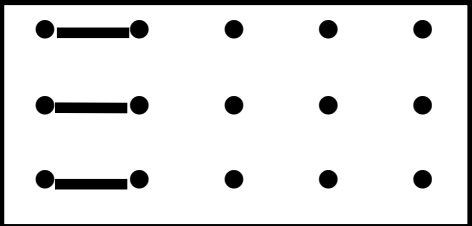
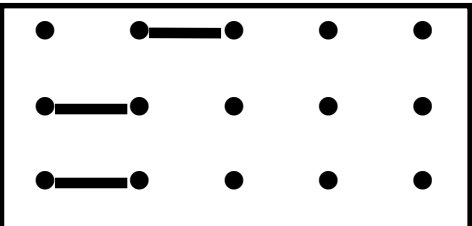
Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	100ns	100ns	100ns
2						14	100ns	100ns	150ns
2						14	100ns	100ns	200ns
2						14	100ns	100ns	250ns



Bank A	Bank B	Bank C
100ns	150ns	100ns

Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	100ns	150ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	150ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	150ns	250ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	200ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	200ns	150ns
	1	4	7	10	13				

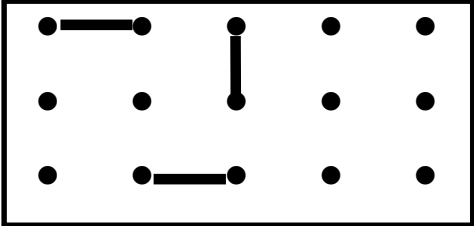
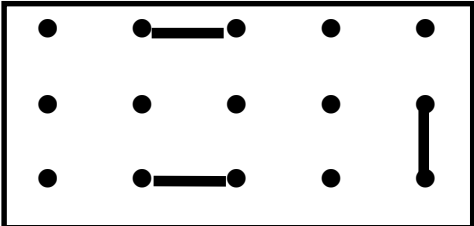
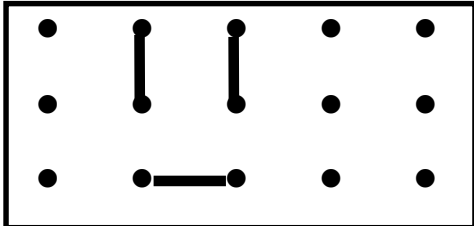
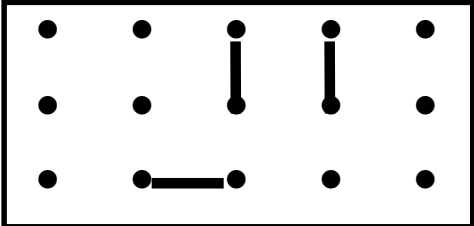
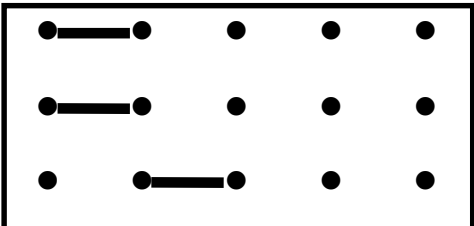
Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	100ns	200ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	200ns	250ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	250ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	250ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	100ns	250ns	200ns
	1	4	7	10	13				

Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	100ns	250ns	250ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	100ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	100ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	100ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	100ns	250ns
	1	4	7	10	13				

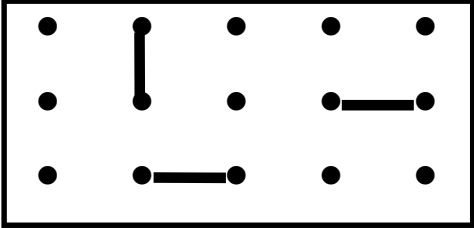
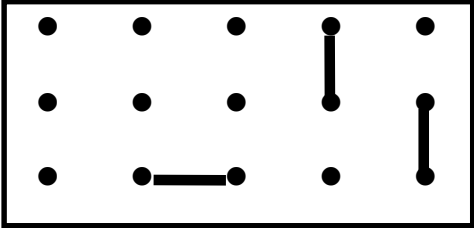
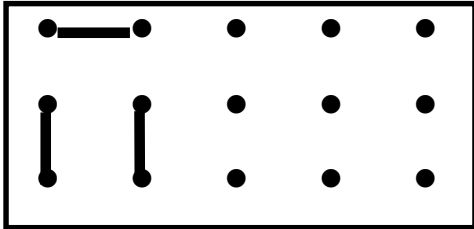
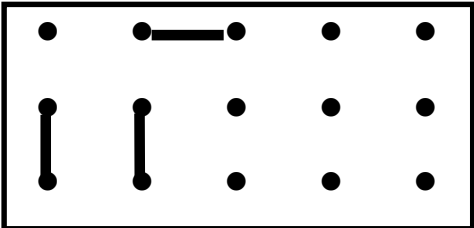
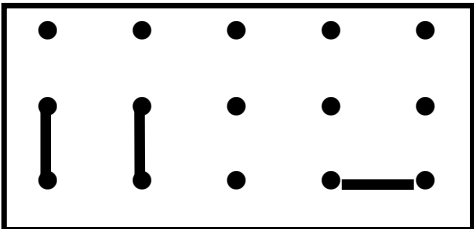
Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	150ns	150ns	100ns
2						14	150ns	150ns	150ns
2						14	150ns	150ns	200ns
2						14	150ns	150ns	250ns
2						14	150ns	200ns	100ns

Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	150ns	200ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	200ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	200ns	250ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	250ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	150ns	250ns	150ns
	1	4	7	10	13				

Jumper ABC configuration for

	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		150ns	250ns	200ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		150ns	250ns	250ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		200ns	100ns	100ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		200ns	100ns	150ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		200ns	100ns	200ns

Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	200ns	100ns	250ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	200ns	150ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	200ns	150ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	200ns	150ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	200ns	150ns	250ns
	1	4	7	10	13				

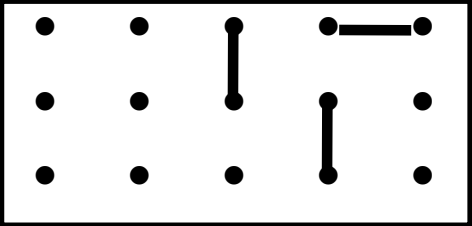
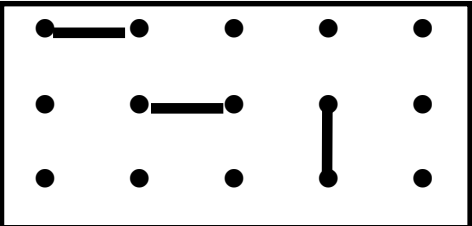
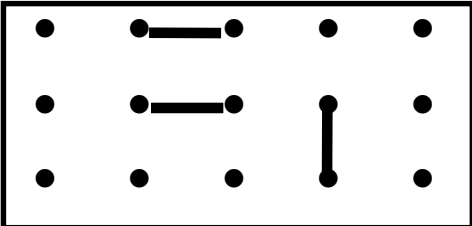
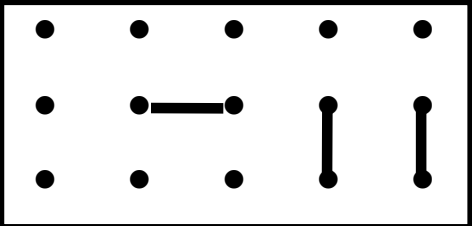
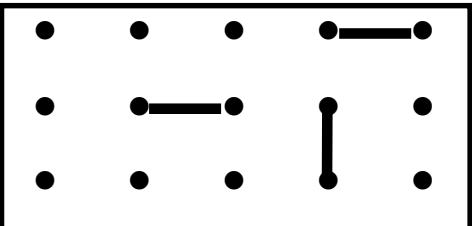
Jumper ABC configuration for

2		14	Bank A	Bank B	Bank C
	<p>3 6 9 12 15</p> <p>1 4 7 10 13</p>		200ns	200ns	100ns
2		14	Bank A	Bank B	Bank C
	<p>3 6 9 12 15</p> <p>1 4 7 10 13</p>		200ns	200ns	150ns
2		14	Bank A	Bank B	Bank C
	<p>3 6 9 12 15</p> <p>1 4 7 10 13</p>		200ns	200ns	200ns
2		14	Bank A	Bank B	Bank C
	<p>3 6 9 12 15</p> <p>1 4 7 10 13</p>		200ns	200ns	250ns
2		14	Bank A	Bank B	Bank C
	<p>3 6 9 12 15</p> <p>1 4 7 10 13</p>		200ns	250ns	100ns

Jumper ABC configuration for

	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		250ns	100ns	200ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		250ns	100ns	250ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		250ns	150ns	100ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		250ns	150ns	150ns
	3	6	9	12	15				
2						14	Bank A	Bank B	Bank C
	1	4	7	10	13		250ns	150ns	200ns

Jumper ABC configuration for

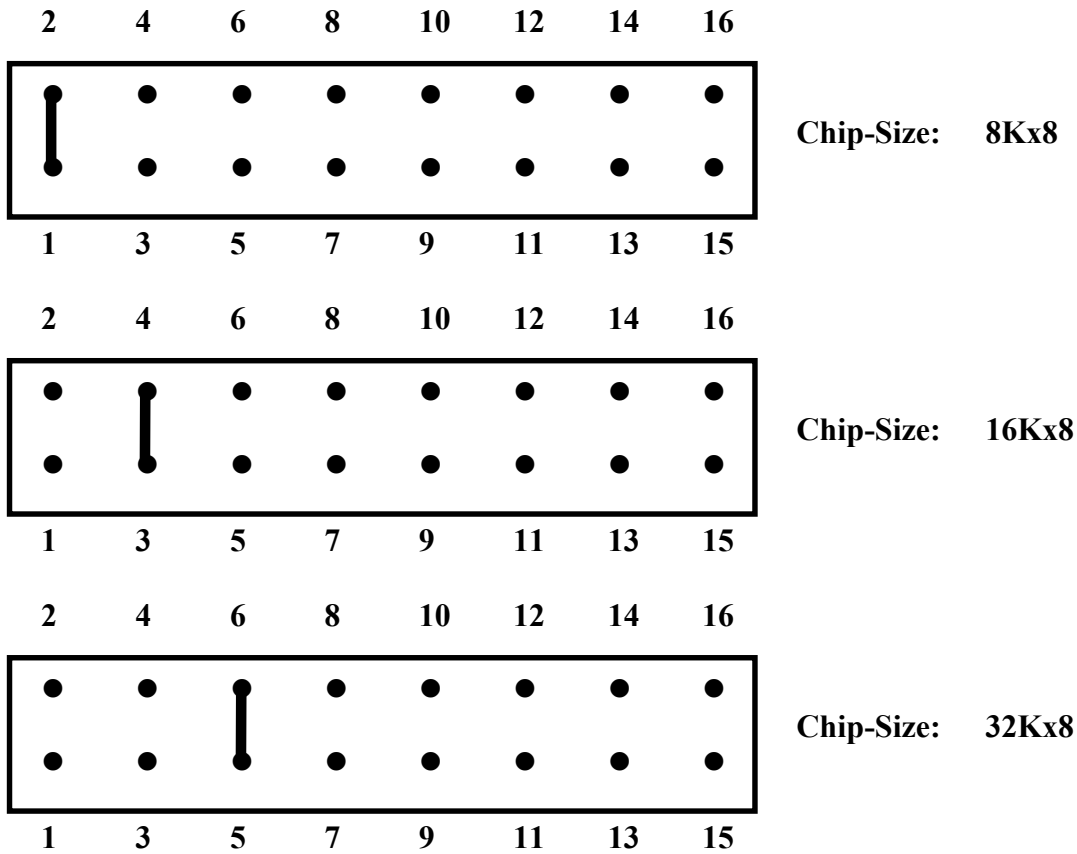
	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	250ns	150ns	250ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	200ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	200ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	200ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	200ns	250ns
	1	4	7	10	13				

Jumper ABC configuration for

	3	6	9	12	15		Bank A	Bank B	Bank C
2						14	250ns	250ns	100ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	250ns	150ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	250ns	200ns
	1	4	7	10	13				
	3	6	9	12	15				
2						14	250ns	250ns	250ns
	1	4	7	10	13				

4.4 Setting of Chip-Size using jumpers AF, BF and CF

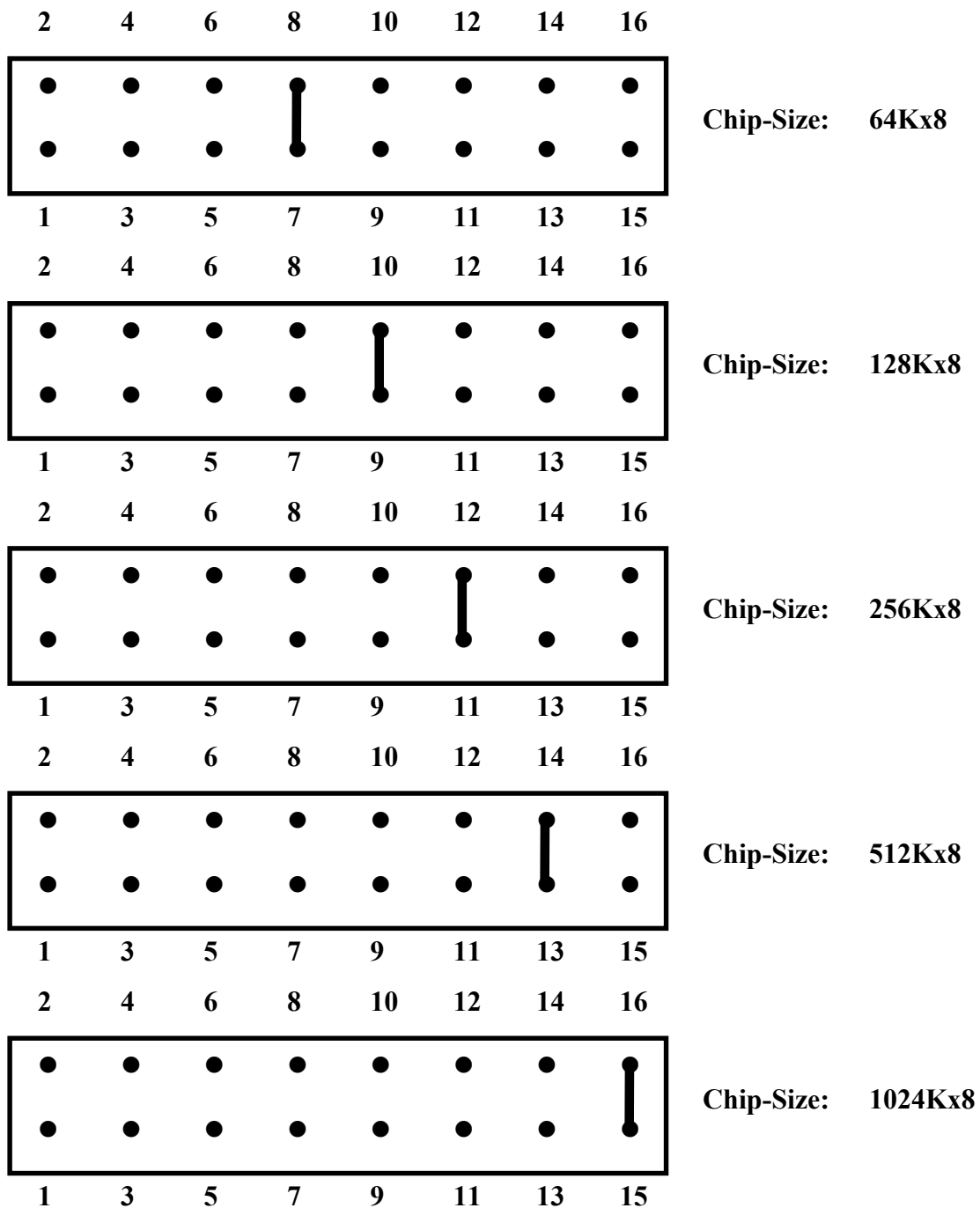
Jumpers AF, BF, CF



Attention! These jumpers are Decoding - Dependant!
Any jumper settings not in accordance with the chip size may not cause any damage, but partial or double decoding will occur!

Jumper AF, BF and CF for used Chip-Size:

Jumpers AF, BF, CF

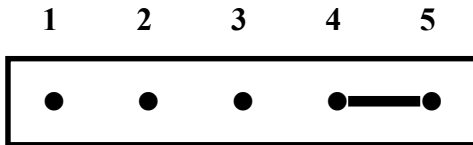


Attention! These jumpers are Decoding-Dependant!
Any jumper settings not in accordance with the chip size may not cause any damage, but partial or double decoding will occur!

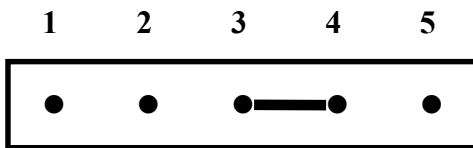
4.5 Base Address Selection using jumpers AC, BC and CC

VME-Address	compared to:	HIGH	LOW	ignored
VME-A15		3-4	4-5	1-2

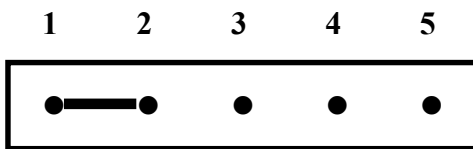
Jumpers AC, BC, CC



for first Bank with 8Kx8 Chips
and the same decoding address
as the second Bank



for second Bank with 8Kx8 Chips
and the same decoding address
as the first Bank

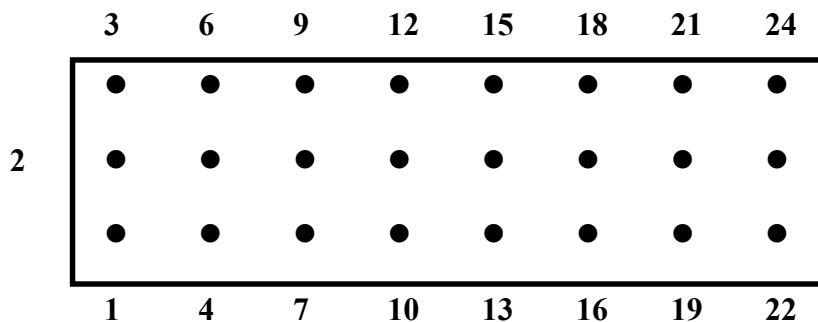


for any Bank with Chips of higher
capacity than 8Kx8

Jumper-Fields AD, BD and CD for Base Address Selection:

VME-Address	compared to :	HIGH	LOW	ignored
VME-A16	---		2-3	1-2
VME-A17	---		5-6	4-5
VME-A18	---		8-9	7-8
VME-A19	---		11-12	10-11
VME-A20	---		14-15	13-14
VME-A21	---		17-18	16-17
VME-A22	---		20-21	19-20
VME-A23	---		23-24	22-23

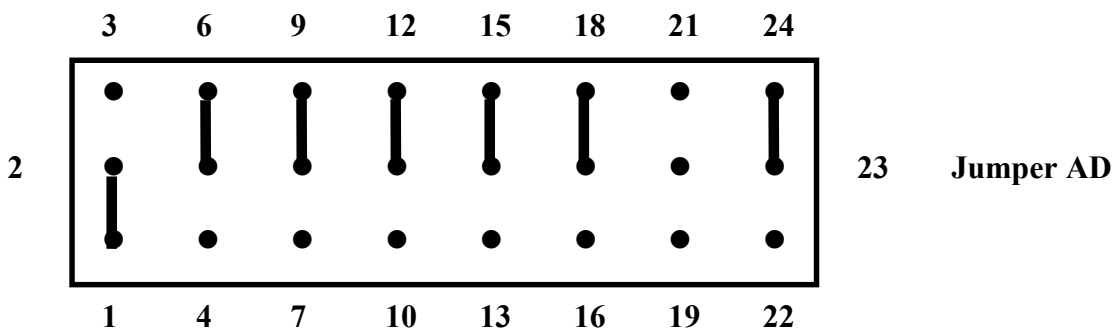
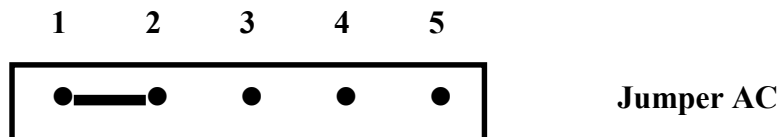
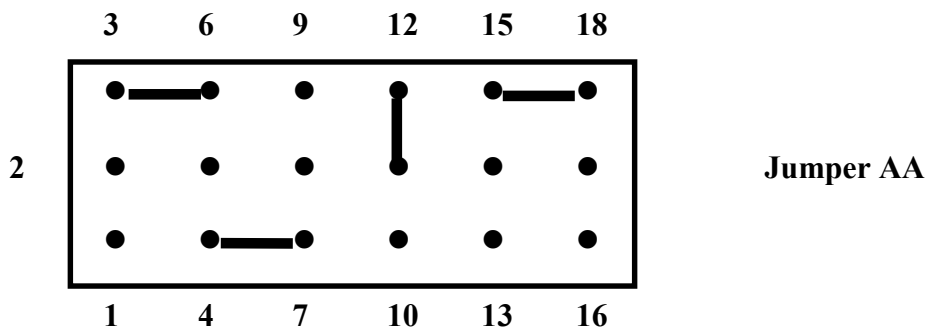
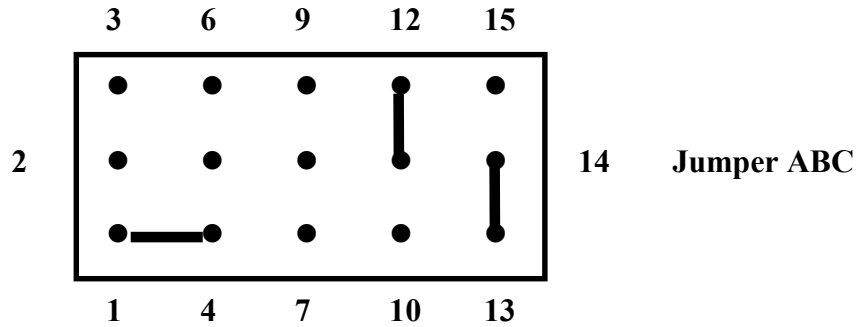
--- = Jumper not installed

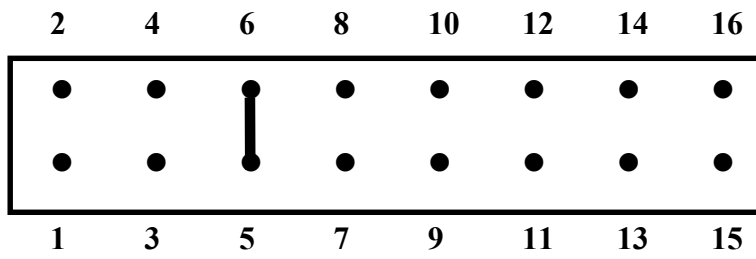


23 Jumper fields
AD, BD, CD

**Example for Address Decoding of Bank A for 40000 H
and 32Kx8 Chips (41256) with 100ns Access Speed
(Bank B & C with 250ns Access Speed)**

Bank-Size : 128KByte
Half-Bank Switching Address : A16
Ignorable lower Addresses : up to A16

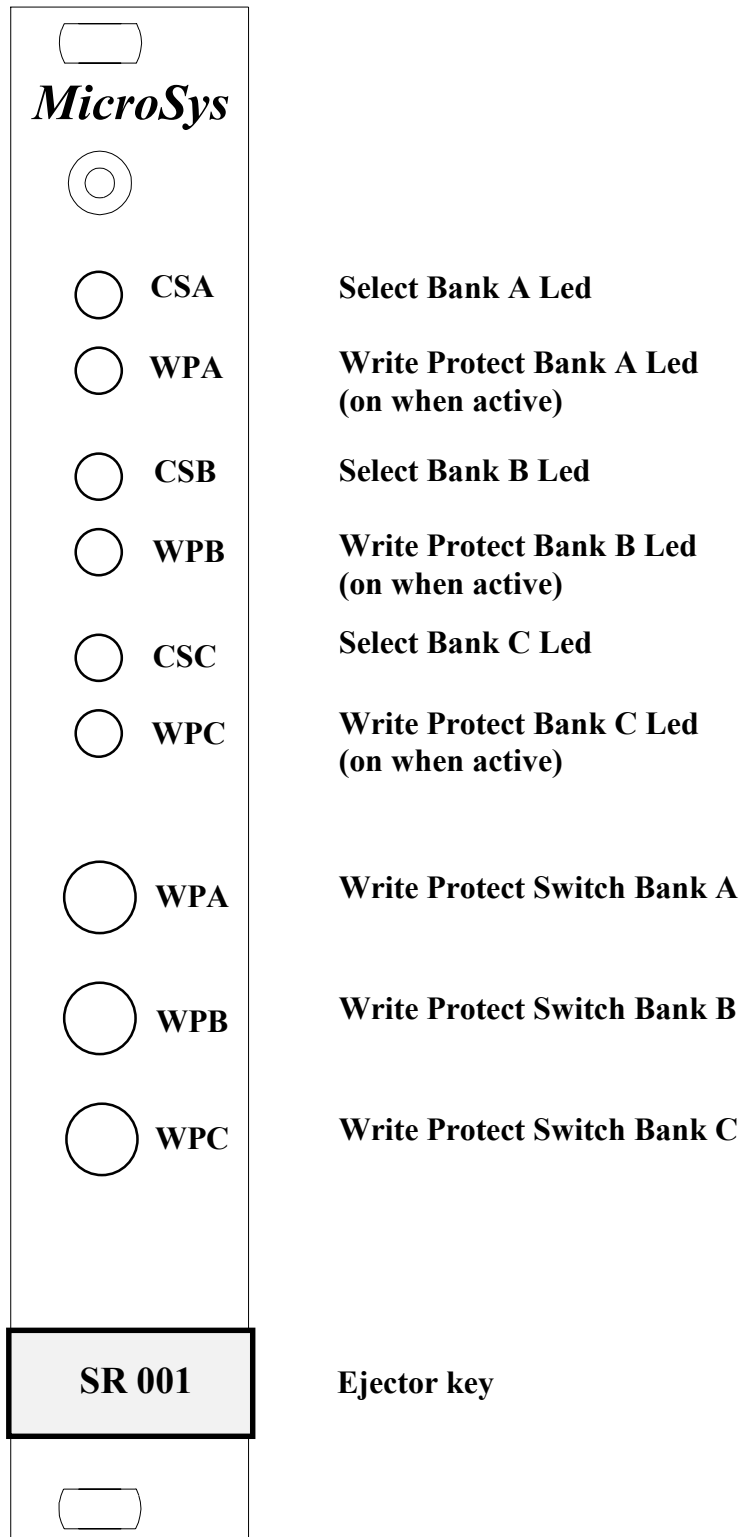




Jumper AF

4.6 Front Panel Description

Figure 1: Front Panel Layout



4.6.1 Front Panel LEDs

- LED1: This led indicates any access to RAM/ROM Bank A, no matter if the current access is inhibited by the write protection. Illegal Accesses made under wrong Address Modifiers are not indicated, because no selection will be performed.
- LED2: If the write protection switch SW1 is in active position, this LED will be illuminated to indicate, that no write accesses can be executed on RAM/ROM Bank A.
- LED3: Works the same as LED1 except for RAM/ROM Bank B.
- LED4: Works the same as LED2 except for RAM/ROM Bank B.
- LED5: Works the same as LED1 except for RAM/ROM Bank C.
- LED6: Works the same as LED2 except for RAM/ROM Bank B.

4.6.2 Front Panel Switches

- SW1: This switch activates in the on-position the write protection facility, which is indicated by LED2. If SW1 is in the off-position, LED2 will be not active and both read and write accesses can be performed on RAM/ROM Bank A.
- SW2: Works the same as SW1 except for RAM/ROM Bank B.
- SW3: Works the same as SW1 except for RAM/ROM Bank C.

4.7 Battery Backup

Each Bank, A, B and C can be protected against data loss by battery backup. This function should only be enabled, if the standby power consumption of the used RAMs is low enough to ensure a suitable time of data retention. Any use with high power chips will not damage onboard circuitry, but shorten the backup time, also depending on the used battery. Any use of this function for ROMs is not necessary and will cause decreasing backup time, because all banks are supplied from one battery source.

There are two different kinds of batteries that can be used: Lithium or NiCd

Caution!

If a 3 volt Lithium-Cell should be installed, the charging resistor R11 must be removed. Lithium Batteries **MUST NOT** be charged!

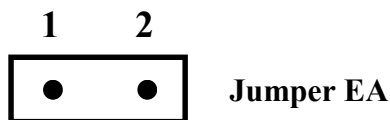
For battery backup with NiCd-Types, three 1,2 volt NiCd-Accumulators must be used. In case of a NiCd-Battery the charging resistor (R11, 3K6, SMD 1206) must be installed.

To enable the battery backup basically, jumper EA must be inserted and a battery must be installed.

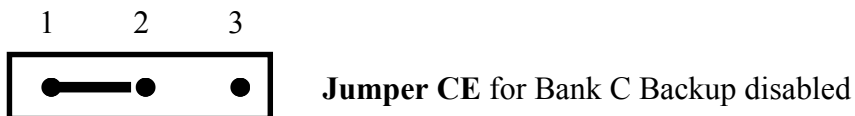
Caution!

Before setting jumper EA, check inserted battery for right polarity!

Jumper EA should be removed, if the board is stored or not used for a longer time, to avoid unintended discharging of the battery.



To enable the battery backup for RAM/ROM Bank A, jumper AE must be set to position 2-3. For normal operation, jumper AE is set to 1-2. RAM/ROM Bank B is connected to the battery backup by jumper BE 2-3, Bank C by jumper CE 2-3. During standard operation these jumpers are handled according to instructions for Bank A.



4.8 VMEbus Interface

The VMEbus-Interface supports all VMEbus-Lines, defined in the VME-Specification Rev.C1. The address bus is 24 bits, the data bus is 16 bits wide. The Connector P1 row A, B, C contains all standard VME-Lines.

The Address Modifier Codes, AM0 to AM5 are a part of the VMEbus-Specifications and serve to differentiate between particular memory areas.

SR 001 accepts the following AM codes:

Table 4-2: AM Codes

AM5	AM4	AM3	AM2	AM1	AM0	Access for	
H	H	H	H	H	L	Standard Superv.Prog.	(3E)
H	H	H	H	L	H	Standard Superv.Data	(3D)
H	H	H	L	H	L	Standard User Prog.	(3A)
H	H	H	L	L	H	Standard User Data	(39)

L = logical low
H = logical high

Jumper DA enables or disables the acceptance of these AM-Codes for each RAM/ROM Bank separately.

DA 1-2 and 3-4 for RAM/ROM/Bank A
DA 5-6 and 7-8 for RAM/ROM/Bank B
DA 9-10 and 11-12 for RAM/ROM/Bank C

Jumper DA			
Bank A	User Mode	1-2	set
	Supervisor Mode	3-4	set
Bank B	User Mode	5-6	set
	Supervisor Mode	7-8	set
Bank C	User Mode	9-10	set
	Supervisor Mode	11-12	set

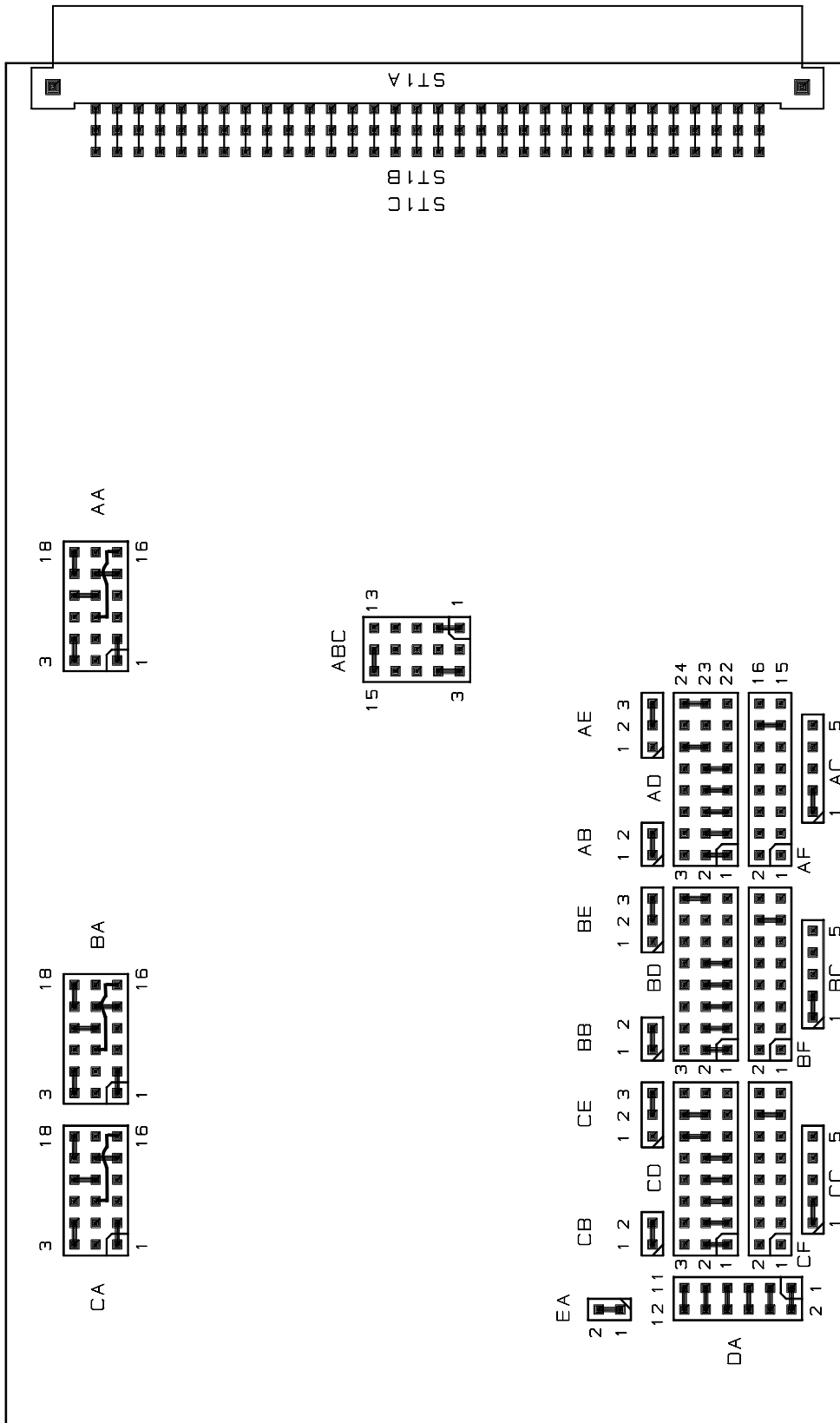
Jumper DA		AM-Codes on:				Bank A	Bank B	Bank C
2	4	6	8	10	12	ignored	ignored	ignored
1	3	5	7	9	11	User	ignored	ignored
2	4	6	8	10	12			
1	3	5	7	9	11	ignored	Supervisor	User
2	4	6	8	10	12			
1	3	5	7	9	11	User	Supervisor	User & Supervisor
2	4	6	8	10	12			

If no jumper of a Bank is installed, the AM-Codes are ignored.

If both jumpers of a bank are installed, User or Supervisor-Access is permitted.

4.9 Default Jumper Settings

(For SRAMs 512K x 8 and address range 0x400000 to 0x9FFFFFF)



4.10 Summary of Jumpers for Bank A

Described function is valid, when jumper is in Position!

Size	Jumper	Position	Function
6x3	AA		Chip-Type RAM/ROM Bank A (set for 512K x 8 SRAM)
1x2	AB	* 1-2	Chip-Type RAM/ROM Bank A
1x5	AC	* 1-2	VME-A15 Bank A not decoded
	AC	2-3	VME-A15 Bank A high decoded
	AC	3-4	VME-A15 Bank A high decoded
	AC	4-5	VME-A15 Bank A low decoded
8x3	AD	* 1-2	VME-A16 Bank A not decoded
	AD	2-3	VME-A16 Bank A low decoded
	AD	---	VME-A16 Bank A high decoded
	AD	* 4-5	VME-A17 Bank A not decoded
	AD	5-6	VME-A17 Bank A low decoded
	AD	---	VME-A17 Bank A high decoded
	AD	* 7-8	VME-A18 Bank A not decoded
	AD	8-9	VME-A18 Bank A low decoded
	AD	---	VME-A18 Bank A high decoded
	AD	* 10-11	VME-A19 Bank A not decoded
	AD	11-12	VME-A19 Bank A low decoded
	AD	---	VME-A19 Bank A high decoded
	AD	* 13-14	VME-A20 Bank A not decoded
	AD	14-15	VME-A20 Bank A low decoded
	AD	---	VME-A20 Bank A high decoded
	AD	16-17	VME-A21 Bank A not decoded
	AD	* 17-18	VME-A21 Bank A low decoded
	AD	---	VME-A21 Bank A high decoded
	AD	19-20	VME-A22 Bank A not decoded
	AD	20-21	VME-A22 Bank A low decoded
	AD	* ---	VME-A22 Bank A high decoded
	AD	22-23	VME-A23 Bank A not decoded
	AD	* 23-24	VME-A23 Bank A low decoded
	AD	---	VME-A23 Bank A high decoded
1x3	AE	1-2	Normal Operation Bank A
	AE	* 2-3	Battery Backup Bank A
7x2	AF	1-2	Chip-Size Bank A = 8Kx8
	AF	3-4	Chip-Size Bank A = 16Kx8
	AF	5-6	Chip-Size Bank A = 32Kx8
	AF	7-8	Chip-Size Bank A = 64Kx8
	AF	9-10	Chip-Size Bank A = 128Kx8
	AF	11-12	Chip-Size Bank A = 256Kx8
	AF	* 13-14	Chip-Size Bank A = 512Kx8
	AF	15-16	Chip-Size Bank A = 1024Kx8

4.11 Summary of Jumpers for Bank B

Described function is valid, when jumper is in Position !

Size	Jumper		Position	Function
6x3	BA			Chip-Type RAM/ROM Bank B (set for 512K x 8 SRAM)
1x2	BB	*	1-2	Chip-Type RAM/ROM Bank B
1x5	BC	*	1-2	VME-A15 Bank B not decoded
	BC		2-3	VME-A15 Bank B high decoded
	BC		3-4	VME-A15 Bank B high decoded
	BC		4-5	VME-A15 Bank B low decoded
8x3	BD	*	1-2	VME-A16 Bank B not decoded
	BD		2-3	VME-A16 Bank B low decoded
	BD		---	VME-A16 Bank B high decoded
	BD	*	4-5	VME-A17 Bank B not decoded
	BD		5-6	VME-A17 Bank B low decoded
	BD		---	VME-A17 Bank B high decoded
	BD	*	7-8	VME-A18 Bank B not decoded
	BD		8-9	VME-A18 Bank B low decoded
	BD		---	VME-A18 Bank B high decoded
	BD	*	10-11	VME-A19 Bank B not decoded
	BD		11-12	VME-A19 Bank B low decoded
	BD		---	VME-A19 Bank B high decoded
	BD	*	13-14	VME-A20 Bank B not decoded
	BD		14-15	VME-A20 Bank B low decoded
	BD		---	VME-A20 Bank B high decoded
	BD		16-17	VME-A21 Bank B not decoded
	BD		17-18	VME-A21 Bank B low decoded
	BD	*	---	VME-A21 Bank B high decoded
	BD		19-20	VME-A22 Bank B not decoded
	BD		20-21	VME-A22 Bank B low decoded
	BD	*	---	VME-A22 Bank B high decoded
	BD		22-23	VME-A23 Bank B not decoded
	BD	*	23-24	VME-A23 Bank B low decoded
	BD		---	VME-A23 Bank B high decoded
1x3	BE		1-2	Normal Operation Bank B
	BE	*	2-3	Battery Backup Bank B
7x2	BF		1-2	Chip-Size Bank B = 8Kx8
	BF		3-4	Chip-Size Bank B = 16Kx8
	BF		5-6	Chip-Size Bank B = 32Kx8
	BF		7-8	Chip-Size Bank B = 64Kx8
	BF		9-10	Chip-Size Bank B = 128Kx8
	BF		11-12	Chip-Size Bank B = 256Kx8
	BF	*	13-14	Chip-Size Bank B = 512Kx8
	BF		15-16	Chip-Size Bank B = 1024Kx8

4.12 Summary of Jumpers for Bank C

Described function is valid, when jumper is in Position!

Size	Jumper		Position	Function
6x3	CA			Chip-Type RAM/ROM Bank C (set for 512K x 8 SRAM)
1x2	CB	*	1-2	Chip-Type RAM/ROM Bank C
1x5	CC	*	1-2	VME-A15 Bank C not decoded
	CC		2-3	VME-A15 Bank C high decoded
	CC		3-4	VME-A15 Bank C high decoded
	CC		4-5	VME-A15 Bank C low decoded
8x3	CD	*	1-2	VME-A16 Bank C not decoded
	CD		2-3	VME-A16 Bank C low decoded
	CD		---	VME-A16 Bank C high decoded
	CD	*	4-5	VME-A17 Bank C not decoded
	CD		5-6	VME-A17 Bank C low decoded
	CD		---	VME-A17 Bank C high decoded
	CD	*	7-8	VME-A18 Bank C not decoded
	CD		8-9	VME-A18 Bank C low decoded
	CD		---	VME-A18 Bank C high decoded
	CD	*	10-11	VME-A19 Bank C not decoded
	CD		11-12	VME-A19 Bank C low decoded
	CD		---	VME-A19 Bank C high decoded
	CD	*	13-14	VME-A20 Bank C not decoded
	CD		14-15	VME-A20 Bank C low decoded
	CD		---	VME-A20 Bank C high decoded
	CD		16-17	VME-A21 Bank C not decoded
	CD	*	17-18	VME-A21 Bank C low decoded
	CD		---	VME-A21 Bank C high decoded
	CD		19-20	VME-A22 Bank C not decoded
	CD	*	20-21	VME-A22 Bank C low decoded
	CD		---	VME-A22 Bank C high decoded
	CD		22-23	VME-A23 Bank C not decoded
	CD		23-24	VME-A23 Bank C low decoded
	CD	*	---	VME-A23 Bank C high decoded
1x3	CE		1-2	Normal Operation Bank C
	CE	*	2-3	Battery Backup Bank C
7x2	CF		1-2	Chip-Size Bank C = 8Kx8
	CF		3-4	Chip-Size Bank C = 16Kx8
	CF		5-6	Chip-Size Bank C = 32Kx8
	CF		7-8	Chip-Size Bank C = 64Kx8
	CF		9-10	Chip-Size Bank C = 128Kx8
	CF		11-12	Chip-Size Bank C = 256Kx8
	CF	*	13-14	Chip-Size Bank C = 512Kx8
	CF		15-16	Chip-Size Bank C = 1024Kx8

4.13 Summary of common Jumpers of Banks A, B & C

Described function is valid, when jumper is in Position!

Size	Jumper	Position	Function
5x3	ABC *	1-4	} Bank A-C 100ns
	ABC *	3-6	
	ABC *	14-15	
6x2	DA *	1-2	Bank A User-Access
	DA *	3-4	Bank A Supervisor-Access
	DA *	5-6	Bank B User-Access
	DA *	7-8	Bank B Supervisor-Access
	DA *	9-10	Bank C User-Access
	DA *	11-12	Bank C Supervisor-Access

Appendices

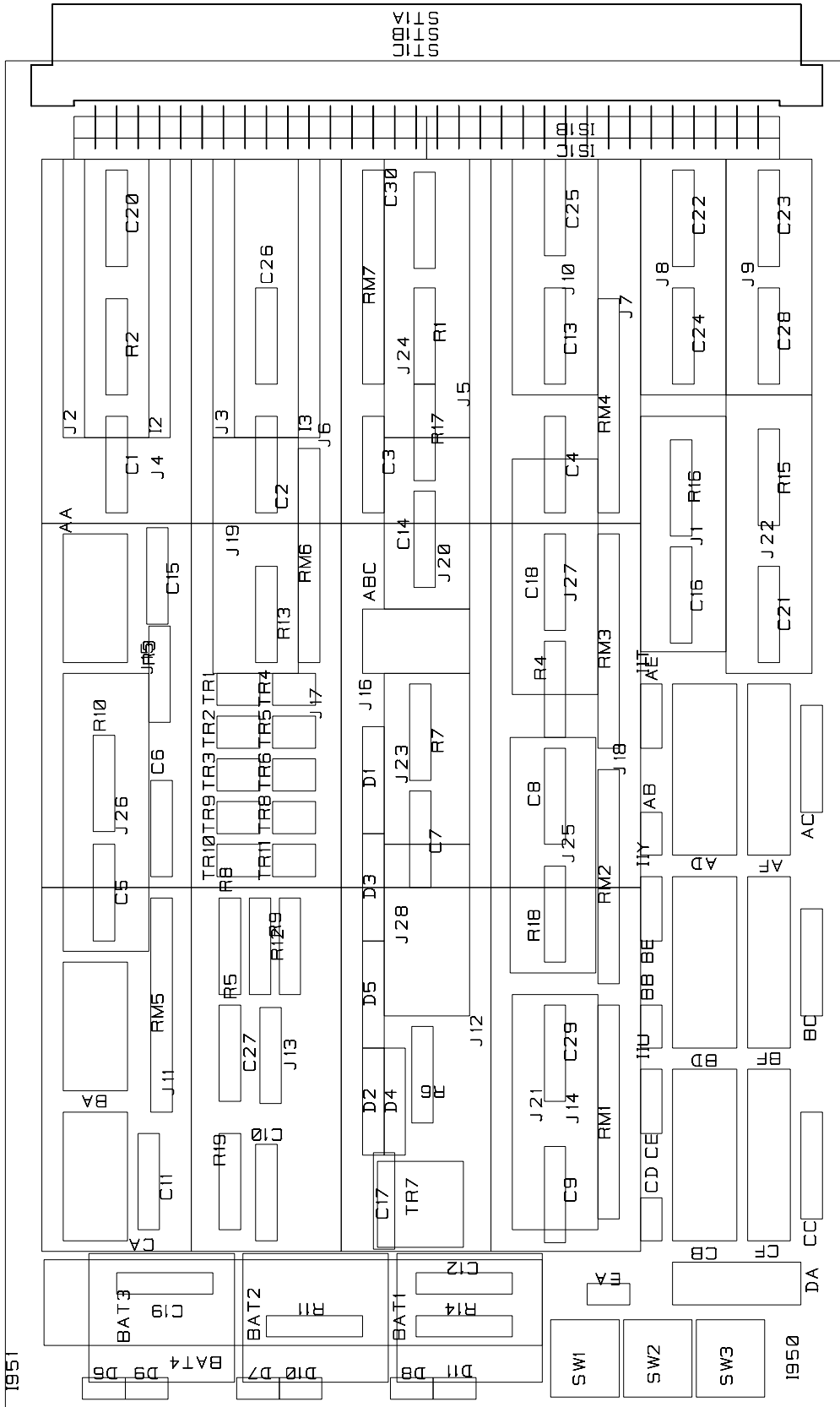
Appendix A: Pin Assignment of VMEbus-Connector P1

Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	---	A17
22	IACKOUT*	---	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	---	+12V
32	+5V	+5V	+5V

Appendix B: Used pins on VMEbus-Connector P1

Pin	Row A	Row B	Row C
1	D00	---	D08
2	D01	---	D09
3	D02	---	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	---	BG3IN*	---
11	GND	BG3OUT*	BERR*
12	DS1*	---	SYSRESET*
13	DS0*	---	LWORD*
14	WRITE*	---	AM5
15	GND	---	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	---	A17
22	IACKOUT*	---	A16
23	AM4	GND	A15
24	A07	---	A14
25	A06	---	A13
26	A05	---	A12
27	A04	---	A11
28	A03	---	A10
29	A02	---	A09
30	A01	---	A08
31	-12V	---	+12V
32	+5V	+5V	+5V

Appendix C: SR 001 Layout Diagram



Appendix D: SR 001 Schematics (in printed versions only)