

Microsys

User's Manual

***miriac*[™] Power Module**

PM854 Rev. 2

3rd edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
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Germany

declare that the product

PM854

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above-mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

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1. Introduction

1.1 Short Description

The **miriac**TM **Power Module PM854** is powered by the Motorola PowerPC **MPC8540**.

It features a **64+8 bit** wide DDR interface for the **128 MByte DDR SDRAM** area **with ECC**. The DDR SDRAM can operate at clock rates up to 166 MHz (DDR333).

The **Flash memory** is connected to the **local bus**, which is 32 bit wide, address/data multiplexed and running at 166 MHz.

External enhancements can be connected to the MPC8540 via the 133 MHz, 64-bit-wide **PCI-X 1.0a/PCI 2.2 Bus** Controller.

The complete **local / PCI-X bus**, the **Rapid I/O interface** and all **I/O lines** of the MPC8540 are accessible by the carrier board through two 200-pin connectors and an additional 100-pin connector.

The communications processor inside the MPC8540 offers one 10/100 MBit/s channel with MII, and two triple-speed 10/100/1000 MBit/s Ethernet interfaces with GMII/TBI/RGMII as well as two 16550-compatible UARTs with RTS/CTS handshake.

The MPC8540 also provides an 8-bit wide RapidIO controller with 500 MHz clock and LVDS signaling, as well as a 4-channel DMA controller and an integrated **Programmable Interrupt Controller**.

The I²C-Interface of the MPC8540 controls a **2KByte EEPROM** and a **RTC** with backup feature.

The MPC8540 works with a 1.2 V core voltage, a 3.3 V I/O and 2.5 V DDR interface supply.

The board is implemented in **CMOS technology** and requires a power supply of 3.3V / **approx. 15 W @ 833 MHz** CPU speed.

1.2 Specifications

The power requirements for the PM854 board are shown in the following table.

Power Requirements:

+3.3V, +5%/-2.5%,	5,0 A (typ. @833 MHz)
-------------------	-----------------------

Environmental Requirements:

Operating Temperature (without forced airflow)	0 ° C to +45 ° C ambient -40°C to +85°C optional) ¹ (Tjunction <105°C)
Relative Humidity	0 to 95 % (non-condensing)
Storage Temperature	-40 ° C to + 85 ° C

)¹ Special heat sink solution necessary for this temperature range

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1.3 Related Documentation

The following manuals are applicable to the PM854:

- MPC8540 Power QUICC-III Microprocessor User's Manual
- DDR SDRAM Data Sheet
- Intel StrataFlash Data Sheet
- PCF8563 Real-Time-Clock User's Manual
- X24C164 EEPROM Data Sheet

2. Delivery

2.1 Items shipped with this unit

- User's Manual PM854 Hardware
- MicroSys shipping carton



ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moist free, dust free environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for PM854 installation

For installation of the PM854, the following items are required.

- Carrier board CR854
- Adequate rated power supply
- Adequate heat sink for processor MPC8540

3.2 Points to be observed

Before the unit is mounted onto the carrier, the following points should be observed.

- Unit requires +3.3V (+ 5 %, - 2,5 %).
- Check default jumper setting.



The operating temperature must never exceed its specified range.

**GUARANTEE IS VOID IF UNIT IS OPERATED
OUT OF Its SPECIFICATIONS!**

3.3 Thermal precautions and heat sink installation

**NEVER RUN THE BOARD WITHOUT PROPERLY INSTALLED
HEAT SINK!
THIS WILL DESTROY THE MPC8540 CPU WITHIN A FEW
SECONDS!**

Use a 1mm thermal pad between the processor and the heat sink and 4mm spacers to fix the heat sink to the PCB. - Take care not to tilt or skew the heat sink while mounting, as this may damage the die!



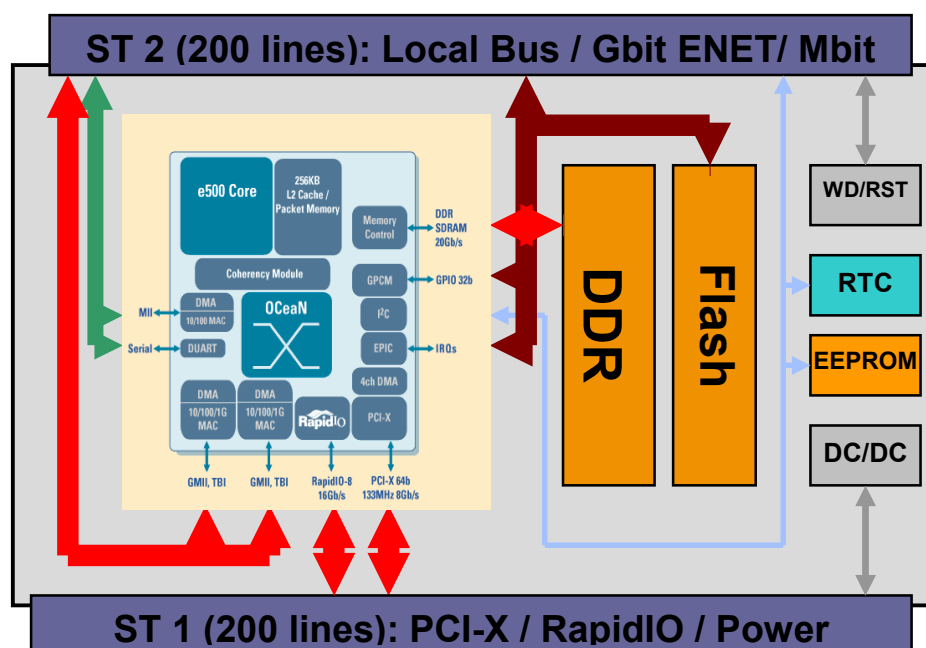
**Attention! The heat sink gets hot when running the PM854 without forced air-cooling!
(Approximately room temperature + 40°C!!)**

4. Board Overview

4.1 Features PM854

Board Format:	95 mm x 80 mm (3.74 inch x 3.15 inch)
Main Processor:	MPC8540 with Embedded e500 Book E compatible Core, 600 MHz to 1 GHz / 1850 MIPS at 800 MHz (est. Dhrystone 2.1) 64 + 8 Bit DDR SDRAM interface with ECC capability, maximum transfer rate DDR333 32 Bit Local Bus (multiplexed address/data) 64 Bit PCI-X 1.0/PCI 2.2 Bus at 133 MHz, 3.3 V only 32 Kbyte L1 instruction cache 32 Kbyte L1 data cache 256 KByte L2 cache 1x MII Interface 10/100 MBit/s 2x GMII/TBI/RGMII Triple-speed interfaces 10/100/1000 MBit/s 2x 16550-compatible UARTs with RTS/CTS handshake
Dynamic RAM:	five DDR-SDRAM devices, DDR333 128MB capacity (optional: 256 MB / 512 MB) 64+8 bit data bus with ECC
Main Flash Memory:	32 MByte capacity with burst capability 32 bit data bus width single 3.3 volt programmable devices
EEPROM:	I ² C serial access device 2KByte capacity
Real Time Clock:	I ² C serial access device PCF8563 with time & date function backup function with onboard gold cap

4.2 Block Diagram



5. Address map PM854

Type	Base	End	Select	Bus	Size
Main DDR SDRAM Bank:					
- Standard 128 MB	\$0000 0000	\$07FF FFFF	CS0	DDR	64Bit
- optional 256 MB	\$0000 0000	\$0FFF FFFF	CS0	DDR	64Bit
- optional 512 MB	\$0000 0000	\$1FFF FFFF	CS0	DDR	64Bit
Flash Bank:					
- Standard 32 MB	\$FE00 0000	\$FFFF FFFF	LCS0	Local Bus	32Bit
- optional 64 MB	\$FC00 0000	\$FFFF FFFF	LCS0	Local Bus	32Bit
Power QUICC-III Internal Memory			---	---	32Bit

Note!

The Address map given is MicroSys default.

All CS areas are programmable, so it may vary with different operating systems.

24C164 EEPROM	\$B0	\$B1	I ² C-Bus
PCF8563 Real Time Clock	\$A2	\$A3	I ² C-Bus

6. Functional Description

6.1 The MPC8540 Processor

The PM854 uses the MPC8540 Power QUICC-III RISC microprocessor from Motorola. It can be configured for different CPU core and bus speed versions. The MPC8540 contains an Embedded e500 Book E compatible core with 32 Kbyte data cache and 32 Kbyte instruction cache. It uses a 3.3V bus supply, a 2.5 V DDR-SDRAM supply and a 1.2 V core supply voltage. The processor works with CPU clock rates up to 1000 MHz and the according system clock rate varies from 66 to 166 MHz.

The PM854 uses a fixed input frequency of 33 MHz. The basic clock configurations can be adjusted via the soldering link area on the bottom side of the PM854, as described in the following section.

6.2 Board configuration

The PM854 has a set of 32 pairs of positions for pull-up/pull-down resistors, which provide the **reset configuration**, i.e. the basic settings of the board.

These are referred to as "pad pair" in the following sections, and are grouped together in several subsections. Their functions are explained in detail in the following chapters.

Each pair of pads can pull one line to either HIGH (CHx link set, CLx link unset) or LOW (CHx link unset, CLx link set).

For example, the pad pair CH1/CL1 belongs to the configuration line "syspll-1", and accordingly inserting the pull-up resistor CH1 will set "syspll-1" to HIGH or logical "1", whereas inserting the pull-down resistor CL1 would set "syspll-1" to LOW or logical 0.

Attention:

- Never insert both links simultaneously on the same line!
- Never use 0 Ohm bridges or solder links, but **ONLY** resistors (recommended value: 4k7) !

The marked line in the tables denotes the default factory setting.

6.2.1 System PLL clock ratio – syspll-[0:3]

These four pad pairs define the clock multiplier ratio for the CCB (Core Complex Bus) clock, based on the system clock.

Line	Pad pair
syspll-0	CH0/CL0
syspll-1	CH1/CL1
syspll-2	CH2/CL2
syspll-3	CH3/CL3

syspll-[0:3]	CCB Clock : SYSCLK Ratio
0001	Reserved
0010	2 : 1
0011	3 : 1
0100	4 : 1
0101	5 : 1
0110	6 : 1
0111	Reserved
1000	8 : 1
1001	9 : 1
1010	10 : 1
1011	Reserved
1100	12 : 1
1101	Reserved
1110	Reserved
1111	Reserved

6.2.2 e500 System Core Clock ratio – corepll-[0:1]

These two pad pairs define the ratio between the e500 core clock and the CCB (Core Complex Bus) clock.

Line	Pad pair
corepll-0	CH4/CL4
corepll-1	CH5/CL5

corepll-[0:1]	e500 Clock : CCB CLK Ratio
00	2 : 1
01	5 : 2
10	3 : 1
11	7 : 2

6.2.3 Boot ROM location – romloc-[0:2]

These three pad pairs define which on-chip peripheral device should be used for booting. Normally, on the PM854 this will be the on-board Flash memory, which is connected to the 32-Bit Local Bus.

Line	Pad pair
romloc-0	CH6/CL6
romloc-1	CH7/CL7
romloc-2	CH8/CL8

romloc-[0:2]	Boot ROM location
000	PCI/PCI-X
001	DDR SDRAM
010	Reserved
011	RapidIO
100	Reserved
101	Local bus GPCM—8-bit ROM
110	Local bus GPCM—16-bit ROM
111	Local bus GPCM—32-bit ROM

6.2.4 Host/Agent Configuration – hostagt-[0:1]

These two pad pairs define whether the MPC8540 acts as a host or an agent on both the RapidIO and the PCI/PCI-X interfaces. Per default, it acts as a host on both interfaces.

Line	Pad pair
hostagt-0	CH9/CL9
hostagt-1	CH10/CL10

hostagt-[0:1]	Host/Agent Configuration
00	MPC8540 acts as an agent of both a PCI/PCI-X and a RapidIO device.
01	MPC8540 acts as an agent of a RapidIO host.
10	MPC8540 acts as an agent of a PCI/PCI-X host.
11	MPC8540 acts as the host processor (default).

6.2.5 External/Internal Boot Configuration – cfgboot

The cfgboot pad pair allows for external configuration of the e500 core by a master CPU before it is allowed to start. The default setting is "1", so the e500 core is allowed to start without prior external configuration and clearance.

Line	Pad pair
cfgboot	CH11/CL11

cfgboot	Boot Configuration
0	CPU boot hold off mode. The e500 core is prevented from booting until configured by an external master.
1	The e500 core is allowed to boot without waiting for configuration by an external master (default).

6.2.6 Boot Sequencer Configuration – cfgseq-[0:1]

The two cfgseq pad pairs determine whether an I²C ROM device should be used for loading the reset configuration instead of reading the hardware (pull-up/pull-down resistor) configuration. By default, this feature is switched off on the PM854.

Line	Pad pair
cfgseq-0	CH12/CL12
cfgseq-1	CH13/CL13

cfgseq-[0:1]	Boot Sequencer Configuration
00	Reserved
01	Normal I ² C addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the I ² C interface. A valid ROM must be present.

cfgseq-[0:1]	Boot Sequencer Configuration
10	Extended I2C addressing mode is used. Boot sequencer is enabled and loads configuration information from a ROM on the I2C interface. A valid ROM must be present.
11	Boot sequencer is disabled. (Default)

6.2.7 TSEC Width Configuration – tsec-width

The tsec-width pad pair determines whether the two TSEC links operate with standard or reduced width.

Line	Pad pair
tsec-width	CH14/CL14

tsec-width	TSEC Width Configuration
0	Ethernet interfaces operate in reduced mode, either RTBI or RGMII, using only four transmit data signals and four receive data signals.
1	Ethernet interfaces operate in their standard TBI or GMII modes using eight transmit data signals and eight receive data signals (default).

6.2.8 TSEC1/ TSEC2 Protocol Configuration – cfmtsec-[1:2]

The cfmtsec-1 and cfmtsec-2 pad pairs determine the protocol for the respective TSEC port.

Line	Pad pair
cfmtsec-1	CH15/CL15
cfmtsec-2	CH16/CL16

cfmtsec-1	TSEC Protocol Configuration
0	The TSEC1 controller operates using the GMII protocol (or RGMII if configured to "reduced mode" with bridge pair CH14/CL14)
1	The TSEC1 controller operates using the TBI protocol (or RTBI if configured to "reduced mode" with bridge pair CH14/CL14)

cfmtsec-2	TSEC Protocol Configuration
0	The TSEC2 controller operates using the GMII protocol (or RGMII if configured to "reduced mode" with bridge pair CH14/CL14)
1	The TSEC2 controller operates using the TBI protocol (or RTBI if configured to "reduced mode" with bridge pair CH14/CL14)

6.2.9 RapidIO Clock Source – rioclk-[0:1]

These two pad pairs define the source of the RapidIO clock.

Line	Pad pair
rioclk-0	CH17/CL17
rioclk-1	CH18/CL18

rioclk-[0:1]	RapidIO Clock Source
00	Reserved
01	The RapidIO receive clock is the source of the transmit clock.
10	The RapidIO transmit clock inputs _____ (RIO_TX_CLK_IN and RIO_TX_CLK) are the source of the transmit clock.
11	The CCB clock is the source of the transmit clock (default).

6.2.10 RapidIO Device ID – dev-ID[5:7]

These three pad pairs define the lower 3 bits of the MPC8540's RapidIO Device ID.

Line	Pad pair
dev-ID5	CH19/CL19
dev-ID6	CH20/CL20
dev-ID7	CH21/CL21

dev-ID[5:7]	RapidIO Device ID
111	Default setting of the MPC8540 Device ID used for RapidIO hosts

6.2.11 PCI Width Configuration – pci-width

The pci-width pad pair determines whether the PCI/PCI-X bus operates in 32-bit or extended 64-bit mode. Default is 32-bit mode.

Line	Pad pair
pci-width	CH22/CL22

pci-width	PCI Width Configuration
0	The PCI/PCI-X interface operates as a 64-bit interface.
1	The PCI/PCI-X interface operates as a 32-bit interface (default).

6.2.12 PCI I/O Impedance – pciimpd

The pciimpd pad pair determines the PCI I/O driver impedance, as shown in the table below. Default is 42 Ohm.

Line	Pad pair
pciimpd	CH23/CL23

pciimpd	PCI I/O Impedance
0	25-Ω I/O drivers are used on the PCI interface.
1	42-Ω I/O drivers are used on the PCI interface (default).

6.2.13 PCI Arbiter Enable – pciarbiter

The pciarbiter pad pair enables or disables the built-in PCI arbiter of the MPC8540. PCI Arbiter is enabled by default.

Line	Pad pair
pciarbiter	CH24/CL24

pciarbiter	PCI Arbiter Enable
0	The on-chip PCI/PCI-X arbiter is disabled. External arbitration is required.
1	The on-chip PCI/PCI-X arbiter is enabled (default).

6.2.14 PCI Debug Mode – pcidebug

The pcidebug pad pair enables or disables the PCI debug mode. In this mode, source ID information is driven onto the highest order address bits PCI_AD[62:58] during the bus command phase (PCI) or attribute phase (PCI-X).

PCI Debug Mode is disabled by default.

Line	Pad pair
pcidebug	CH25/CL25

pcidebug	PCI Debug Mode
0	PCI debug is enabled. Source ID information is driven onto the highest order address bits, PCI_AD[62:58], during the bus command phase (PCI) or attribute phase (PCI-X).
1	PCI operates in normal mode (default).

6.2.15 PCI/PCI-X Mode Selection – pcimode

The pcimode pad pair switches between PCI and PCI-X mode. Default is PCI mode.

Line	Pad pair
pcimode	CH26/CL26

pcimode	PCI/PCI-X Mode Selection
0	PCI-X Mode
1	PCI mode (default).

6.2.16 Memory Debug Mode – memdebug

The memdebug pad pair selects the memory port from which debug information will be driven to the MSRCID and MDVAL signals. Per default, the DDR SDRAM is selected for debug information.

Line	Pad pair
memdebug	CH27/CL27

memdebug	Memory Debug Mode
0	Debug information from the local bus controller (LBC) is driven on the MSRCID and MDVAL signals
1	Debug information from the DDR SDRAM Controller is driven on the MSRCID and MDVAL signals.

6.2.17 DDR Debug Mode – ddrdebug

The ddrdebug pad pair enables or disables a DDR memory controller debug mode in which the DDR SDRAM source ID field and data valid strobe are driven onto the ECC pins. ECC checking and generation are disabled in this case. Per default, the DDR debug mode is switched off, and the ECC lines function normally.

Line	Pad pair
ddrdebug	CH28/CL28

ddrdebug	DDR Debug Mode
0	Debug information is driven on the ECC pins instead of normal ECC I/O. ECC signals from memory devices must be disconnected!!
1	Debug information is not driven on ECC pins. ECC pins function in their normal mode (default).

6.2.18 PCI/PCI-X Output Hold Configuration – pcihold-[0:1]

The two pcihold pad pairs select the output hold times on the PCI or PCI-X bus. **These timings differ between PCI and PCI-X specification**, so these bridges have different meanings depending on the chosen bus type. For details on timing settings, see the *MPC8540 Integrated Processor Hardware Specifications*.

Line	Pad pair
pcihold-0	CH29/CL29
pcihold-1	CH30/CL30

pcihold-[0:1]	PCI Mode Output Hold Configuration
00	One added buffer delay (default + 3 mod 4)
01	Zero added buffer delays (default + 2 mod 4)
10	Three added buffer delays (default + 1)
11	Two added buffer delays—required to meet 2-ns hold time requirement

pcihold-[0:1]	PCI-X Mode Output Hold Configuration
00	Three added buffer delays (default + 3)
01	Two added buffer delays (default + 2)
10	One added buffer delay (default + 1)
11	Zero added buffer delays—meets 0.7 ns hold time requirement

6.2.19 Local Bus Output Hold Configuration – lbhold-[0:1]

The two lbhold pad pairs select the output hold times on the local bus. For details on timing settings, see the *MPC8540 Integrated Processor Hardware Specifications*.

Line	Pad pair
lbhold-0	CH31/CL31
lbhold-1	CH32/CL32

lbhold-[0:1]	Local Bus Output Hold Configuration
00	Zero added buffer delays (zero added buffer delays for LALE)
01	Three added buffer delays (default + 2) (one added buffer delay for LALE)
10	Two added buffer delays (default + 1) (one added buffer delay for LALE)
11	One added buffer delay (default) (zero added buffer delays for LALE)

6.3 The JTAG/COP interface

The **JTAG/COP** interface of the PM854 can only be used via the carrier board. The 200-pin SMD connector ST2 contains the necessary lines according to the following table.

ST2 pin	Signal	Signal	ST2 pin
1	GND	GND	2
3	<i>STDBY</i>	<i>KRST#</i>	4
5	SRST#	HRST#	6
7	<i>HRSO#</i>	TRST#	8
9	TMS	TCK	10
11	TDO	TDI	12
13	CKSTO	CKSTI	14

6.4 Memory

6.4.1 The Main DRAM Area with ECC

The PM854 is fitted with five synchronous dynamic ram devices, which allows for a total capacity of 128 MByte or – optionally – 256 or 512 MByte depending on the used chip sizes. The MPC8540 has an integrated DDR SDRAM controller, which provides all necessary signaling. The DDR SDRAM data port is 64 bits wide, along with 8 ECC bits. The DDR SDRAM contains 4 banks and supports auto refresh and self refresh. It is organized with 13 row and 10 column addresses. The pins of the DDR SDRAM devices are controlled by the MPC8540 according to the following table.

DDR SDRAM	MPC8540	Description
A0-A12	MA0-MA12	DDR SDRAM address port
D0-D63	MDQ0-MDQ63	DDR SDRAM data port
BA0-BA1	MBA0-MBA1	Bank Select
UDM, LDM	MDM0-MDM7	Byte Selects
UDQS, LDQS	MQS0-MQS7	Data Stobes
RAS#	MRAS#	Row Address Strobe
CAS#	MCAS#	Column Address Strobe
CS#	MCS0#	Chip Select
WE#	MWE#	Write Enable



For detailed information about the SDRAM chip specification, please refer to the according SDRAM data sheet.

6.4.2 The Main Flash Memory

The main flash memory area of the PM854 consists of two Intel StrataFlash devices with a total capacity of 32 Mbyte or – optional – 64 MByte. The 32 bit wide main flash bank can be controlled via the LCS0# line on the local 32-bit bus of the MPC8540, and no parity check is performed. The addresses and data are multiplexed on the 8540's local bus, so the addresses have to be demultiplexed by external address latches.

The WAIT pin is not connected and left floating, and so is the ADV pin. For write protection of the Flash, the VPEN pin of both devices can be connected to ground via soldering link FWPT. The pins of the Flash devices are controlled by the MPC8540 according to following table.

Main Flash Bank	MPC8540	Description
A1-A24	LA29-LA6	demultiplexed addresses
D0-D31	LAD0-LAD31	Local Bus data
CE0#	LCS0#	Local Bus CS0#
CE1#, CE2#	GND	Ground
OE#	LGPL2	Output Enable
WE#	LWE2#	Write Enable
RP/RST#	FRST#	Flash Reset
VPEN	VPEN	Flash Program Enable
STS	STS	Flash Status
BYTE#	VDD	
WAIT,ADV,CLK	open	

6.4.3 Boot Options

Usually the PM854 will boot from the main Flash area. However, it is possible to use a different boot configuration, selectable by the **romloc-[0:2] pads**, e.g. to boot from a PCI device, or to have a Master CPU load the boot code into the SDRAM and let the MPC8540 boot from RAM.

The **cfgseq** pad pairs select if the rest of the reset configuration is read from the pull-up/pull-down resistor combinations (default) or from the serial EEPROM.

6.4.3.1 Flash Address Map

The Flash memory is organized in 128 equally sized blocks of 64K x 16-bit Words per part, resulting in 128 x 64K LWords total (32 MB) in the standard configuration.

Optionally, it can be equipped with the double amount, i.e. 256 x 64K LWords total (64 MB).

The address range is from \$FE000000 to \$FFFFFFF (standard, 32 MB), or \$FC000000 to \$FFFFFFF (optional, 64 MB). The boot code resides at \$FFF00000 in the MicroSys standard configuration.

6.5 The I²C Bus

The I²C bus onboard the PM854 is controlled via the SDA and SCL pins of the MPC8540 and contains a real-time clock and an EEPROM. The I²C is made available on ST2, pins 17 (SDA) and 19 (SCL) for further use via the carrier board. Both lines are equipped with 10k pull-up resistors.

6.5.1 The EEPROM

The PM854 offers a 16KBit serial EEPROM for storing system or board parameters. The X24C164 device is internally organized to 2048 x 8 bit and allows for at least 100000 write cycles with a typical cycle time of 5ms.

The 24C164 device responds on the I²C bus at address \$B1 for read and \$B0 for write accesses.



**For detailed programming information and chip description,
please refer to X24C164 Data Sheet !**

6.5.2 The Real Time Clock

The PCF8563 RTC features a clock function with a calendar and a universal timer with alarm and interrupt function. The RTC is protected against data loss by a backup circuitry. The backup feature supplied from a service free gold capacitor cannot be disabled. For long time applications the standby line on ST2 pin 3 can be used to supply the necessary backup power.

The RTC device responds on the I²C bus at address \$A3 for read and \$A2 for write accesses.



**For detailed programming information and chip description,
please refer to Philips PCF8563 Data Sheet !**

6.6 Miscellaneous

6.6.1 The Backup Feature

The backup feature of the PM854 is used to protect the **RTC** against data loss. The backup supply is provided by a **service free gold capacitor**, which is charged by both the VDD supply and the external STDBY line of connector ST2. The RTC cannot be disconnected from the backup power.

The gold capacitor allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended the backup power can be supplied via the standby line on connector ST2, pin 3. The external supply voltage should not exceed 3.6 volts and not fall below 2.5 volts to ensure correct data retention.

6.6.2 The Board Reset and Watchdog Function

During power up or power down sequences, the combination of MAX823 and MAX811 ICs provide correct reset sequencing for the Flash and the CPU. The CPU reset line will be held low for at least 200ms if the supply voltage reaches 3.0 volts. Below that voltage, the reset line will be continuously low.

The watchdog function is realized by a RS flip-flop and a watchdog timer circuit, which controls the board HRST# reset line. The watchdog start and retrigger function is accomplished by the CSWD# line, which is available on the connector ST2, pin 143. This trigger line is low active, has an onboard 10K pull-up and is not driven by any onboard source. In case the watchdog function should be used, a connection to a low active toggle source must be realized via the carrier board. The toggle source can be any signal which is able to issue a state change at least every 1.12 seconds with a minimum pulse width of 50ns. Once a low active pulse has been detected by the watchdog circuitry, it cannot be disabled by any other function than a board reset. If the CSWD# pin is left unconnected, the watchdog function is disabled. The signal high level must never exceed 3.3V and the signal low level must reach at least 0.7V.

6.7 The PM854 Interrupt Structure

There are 12 low active interrupt lines onboard the PM854. None of them is used on-board, so they are all available for off-board circuitry. The interrupt levels are assigned according to the following table.

Level	MPC8540	External Source
0	IRQ0#	not used, ST1 pin13
1	IRQ1#	not used, ST1 pin15
2	IRQ2#	not used, ST1 pin17
3	IRQ3#	not used, ST1 pin19
4	IRQ4#	not used, ST1 pin 21
5	IRQ5#	not used, ST1 pin 23
6	IRQ6#	not used, ST1 pin 14
7	IRQ7#	not used, ST1 pin 16
8	IRQ8#	not used, ST1 pin 18
9	IRQ9# / DREQ3#	not used, ST1 pin 20
10	IRQ10# / DACK3#	not used, ST1 pin 22
11	IRQ11# / DONE3#	not used, ST1 pin 24

6.8 The Board Connectors

The PM854 uses two 200-pin connectors and one 100-pin connector to link all power, bus and communication lines to the carrier board.

6.8.1 Pin Assignment - Connector ST1 (200 pins)

Pin	Signal	Signal	Pin
1	ground	ground	2
3	VDD	VDD	4
5	VDD	VDD	6
7	VDD	VDD	8
9	VDD	VDD	10
11	ground	ground	12
13	IRQ0#	IRQ6#	14
15	IRQ1#	IRQ7#	16
17	IRQ2#	IRQ8#	18
19	IRQ3#	IRQ9#	20
21	IRQ4#	IRQ10#	22
23	IRQ5#	IRQ11#	24
25	n.c.	IOUT#	26
27	n.c.	n.c.	28
29	ground	ground	30
31	RIO-RD1	RIO-RD0	32
33	RIO-RD1#	RIO-RD0#	34
35	RIO-RD3	RIO-RD2	36
37	RIO-RD3#	RIO-RD2#	38
39	ground	ground	40
41	RIO-RCK	RIO-RCK#	42
43	ground	ground	44
45	RIO-RD5	RIO-RD4	46
47	RIO-RD5#	RIO-RD4#	48
49	RIO-RD7	RIO-RD6	50
51	RIO-RD7#	RIO-RD6#	52
53	ground	ground	54
55	RIO-RFR#	RIO-RFR	56
57	ground	ground	58
59	RIO-TCKI#	RIO-TCKI	60
61	ground	ground	62
63	RIO-TFR#	RIO-TFR	64
65	ground	ground	66
67	RIO-TD7#	RIO-TD6	68
69	RIO-TD7	RIO-TD6#	70

pin assignment of the connector ST1 continued

pin assignment of the connector ST1 continued

Pin	Signal	Signal	Pin
71	RIO-TD5#	RIO-TD4#	72
73	RIO-TD5	RIO-TD4	74
75	ground	ground	76
77	RIO-TCK#	RIO-TCK	78
79	ground	ground	80
81	RIO-TD3#	RIO-TD2#	82
83	RIO-TD3	RIO-TD2	84
85	RIO-TD1	RIO-TD0#	86
87	RIO-TD1#	RIO-TD0	88
89	ground	ground	90
91	n.c.	n.c.	92
93	CCKO	PCICLK	94
95	ground	ground	96
97	REQ64#	ACK64#	98
99	PERR#	PAR64	100
101	STOP#	SERR#	102
103	IDSEL	PAR	104
105	DVSL#	IRDY#	106
107	FRME#	TRDY#	108
109	ground	ground	110
111	AD7	AD39	112
113	AD6	AD38	114
115	AD5	AD37	116
117	AD4	AD36	118
119	AD3	AD35	120
121	AD2	AD34	122
123	AD1	AD33	124
125	AD0	AD32	126
127	CBE0#	CBE4#	128
129	AD15	AD47	130
131	AD14	AD46	132
133	AD13	AD45	134
135	AD12	AD44	136
137	AD11	AD43	138
139	AD10	AD42	140
141	AD9	AD41	142
143	AD8	AD40	144
145	CBE1#	CBE5#	146
147	ground	ground	148
149	AD23	AD55	150
151	AD22	AD54	152
153	AD21	AD53	154

pin assignment of the connector ST1 continued

pin assignment of the connector ST1 continued

Pin	Signal	Signal	Pin
155	AD20	AD52	156
157	AD19	AD51	158
159	AD18	AD50	160
161	AD17	AD49	162
163	AD16	AD48	164
165	CBE2#	CBE6#	166
167	AD31	AD63	168
169	AD30	AD62	170
171	AD29	AD61	172
173	AD28	AD60	174
175	AD27	AD59	176
177	AD26	AD58	178
179	AD25	AD57	180
181	AD24	AD56	182
183	CBE3#	CBE7#	184
185	ground	ground	186
187	GNT4#	n.c.	188
189	REQ4#	n.c.	190
191	GNT2#	GNT3#	192
193	REQ2#	REQ3#	194
195	GNT0#	GNT1#	196
197	REQ0#	REQ1#	198
199	ground	ground	200

6.8.2 Pin Assignment - Connector ST2 (200 pins)

Pin	Signal	Signal	Pin
1	ground	ground	2
3	STDBY	KRST#	4
5	SRST#	HRST#	6
7	HRSO#	TRST#	8
9	TMS	TCK	10
11	TDO	TDI	12
13	CKSTO	CKSTI	14
15	n.c.	ASLEEP	16
17	SDA	TRGI	18
19	SCL	TRGO	20
21	THERM0	THERMI	22
23	CTS0	CTS1	24
25	RTS0	RTS1	26
27	TXD0	TXD1	28
29	RXD0	RXD1	30
31	ground	ground	32
33	EC0-COL	EC0-CRS	34
35	EC0-TD3	EC0-RD3	36
37	EC0-TD2	EC0-RD2	38
39	EC0-TD1	EC0-RD1	40
41	EC0-TD0	EC0-RD0	42
43	EC0-TXE	EC0-RDV	44
45	EC0-TXR	EC0-RXR	46
47	EC0-TXC	EC0-RXC	48
49	ground	ground	50
51	EC2-TD5	EC2-TD0	52
53	EC2-TD6	EC2-TD1	54
55	EC2-TD7	EC2-TD2	56
57	EC2-TXE	EC2-TD3	58
59	EC2-TXR	EC2-TD4	60
61	EC2-TXC	n.c.	62
63	n.c.	EC2-CRS	64
65	EC2-COL	ground	66
67	ground	EC2-RD5	68
69	EC2-RD0	EC2-RD6	70
71	EC2-RD1	EC2-RD7	72
73	EC2-RD2	EC2-RDV	74
75	EC2-RD3	EC2-RXR	76
77	EC2-RD4	EC2-RXC	78
79	ground	ground	80

pin assignment of connector ST2 continued

pin assignment of connector ST2 continued

Pin	Signal	Signal	Pin
81	EC2-GXC	EC1-GXC	82
83	ground	ground	84
85	EC1-TD5	EC1-TD0	86
87	EC1-TD6	EC1-TD1	88
89	EC1-TD7	EC1-TD2	90
91	EC1-TXE	EC1-TD3	92
93	EC1-TXR	EC1-TD4	94
95	EC1-TXC	ground	96
97	ground	EC1-CRS	98
99	EC1-COL	n.c.	100
101	n.c.	EC1-RD5	102
103	EC1-RD0	EC1-RD6	104
105	EC1-RD1	EC1-RD7	106
107	EC1-RD2	EC1-RDV	108
109	EC1-RD3	EC1-RXR	110
111	EC1-RD4	EC1-RXC	112
113	n.c.	ground	114
115	ground	EC-MDCK	116
117	EC-GTCK	EC-MDIO	118
119	ground	ground	120
121	LCLK0	LCLK0	122
123	LCLK1	LCLK2	124
125	ground	ground	126
127	LDP1	LDP0	128
129	LDP3	LDP2	130
131	DRQ0#	BA27	132
133	DAC0#	BA28	134
135	DON0#	BA29	136
137	DRQ1#	BA30	138
139	DAC1#	BA31	140
141	DON1#	LGPL0	142
143	CSWD#	LGPL1	144
145	LAL0	LGPL2	146
147	LCS0#	LGPL3	148
149	LCS1#	LGPL4	150
151	LCS2#	LGPL5	152
153	LCS3#	LBCTL	154
155	LCS4#	LWE0#	156
157	LCS5#	LWE1#	158
159	LCS6#	LWE2#	160
161	LCS7#	LWE3#	162
163	ground	ground	164

pin assignment of connector ST2 continued

pin assignment of connector ST2 continued

Pin	Signal	Signal	Pin
165	LAD0	LAD16	166
167	LAD1	LAD17	168
169	LAD2	LAD18	170
171	LAD3	LAD19	172
173	LAD4	LAD20	174
175	LAD5	LAD21	176
177	LAD6	LAD22	178
179	LAD7	LAD23	180
181	ground	ground	182
183	LAD8	LAD24	184
185	LAD9	LAD25	186
187	LAD10	LAD26	188
189	LAD11	LAD27	190
191	LAD12	LAD28	192
193	LAD13	LAD29	194
195	LAD14	LAD30	196
197	LAD15	LAD31	198
199	ground	ground	200

6.8.3 Pin Assignment - Connector ST3 (100 pins)

This connector is mounted on PM856 boards with MPC8560 processor only!

Pin	Signal	Signal	Pin
1	ground	PC0	2
3	PA0	PC1	4
5	PA1	PC2	6
7	PA2	PC3	8
9	PA3	PC4	10
11	PA4	PC5	12
13	PA5	PC6	14
15	PA6	PC7	16
17	PA7	PC8	18
19	PA8	PC9	20
21	PA9	PC10	22
23	PA10	PC11	24
25	PA11	PC12	26
27	PA12	PC14	28
29	PA13	PC16	30
31	PA14	PC19	32
33	PA15	PC20	34
35	PA16	PC21	36
37	PA17	PC22	38
39	PA18	PC23	40
41	PA19	PC24	42
43	PA20	PC25	44
45	PA21	PC26	46
47	PA22	PC27	48
49	PA23	PC28	50
51	PA24	PC29	52
53	PA25	PC30	54
55	PA26	PC31	56
57	PA27	ground	58
59	PA28	PD4	60
61	PA29	PD5	62
63	PA30	PD6	64
65	PA31	PD7	66
67	ground	PD8	68
69	PB18	PD9	70
71	PB19	PD10	72
73	PB20	PD11	74
75	PB21	PD12	76
77	PB22	PD13	78

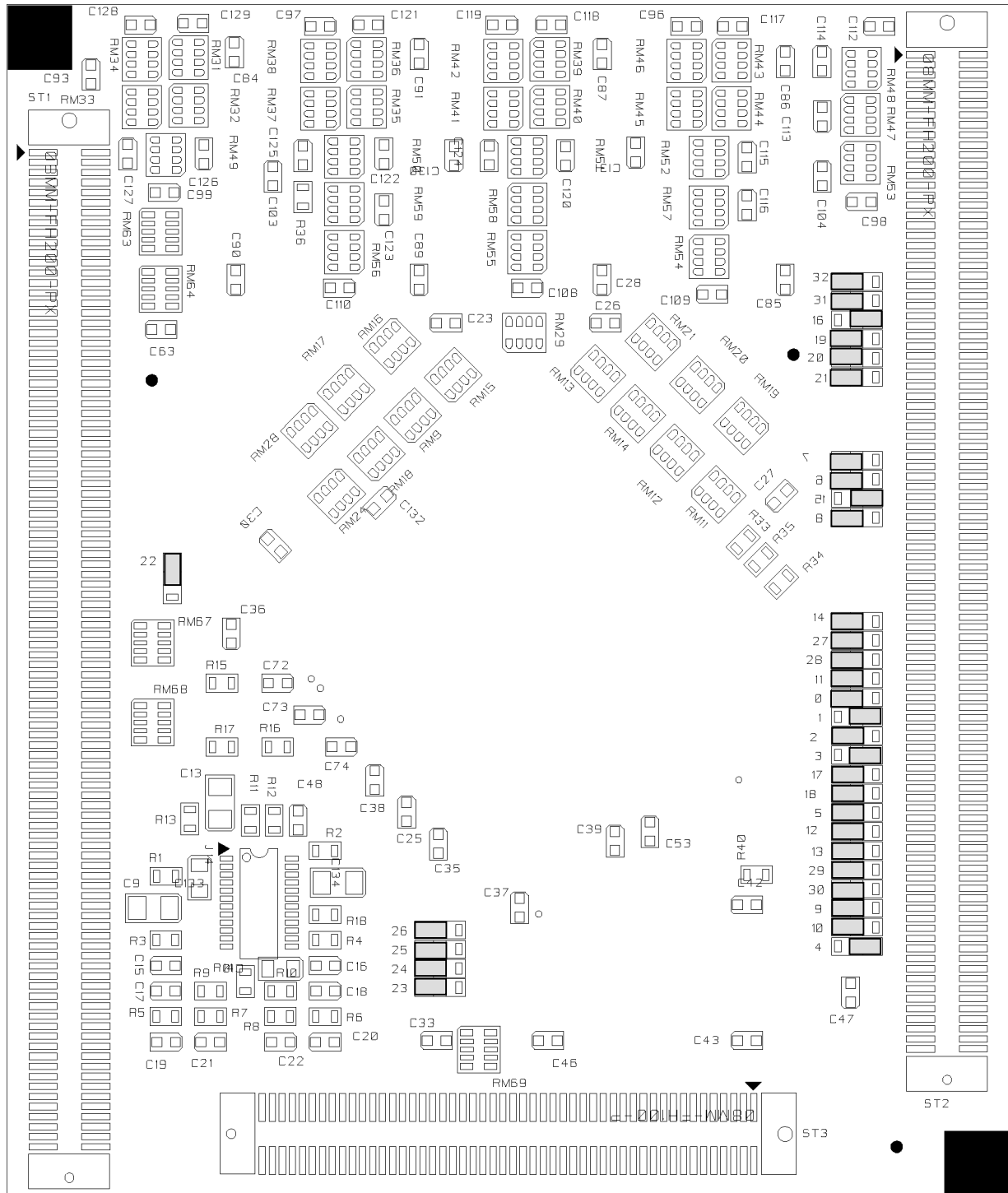
pin assignment of connector ST3 continued

pin assignment of connector ST3 continued

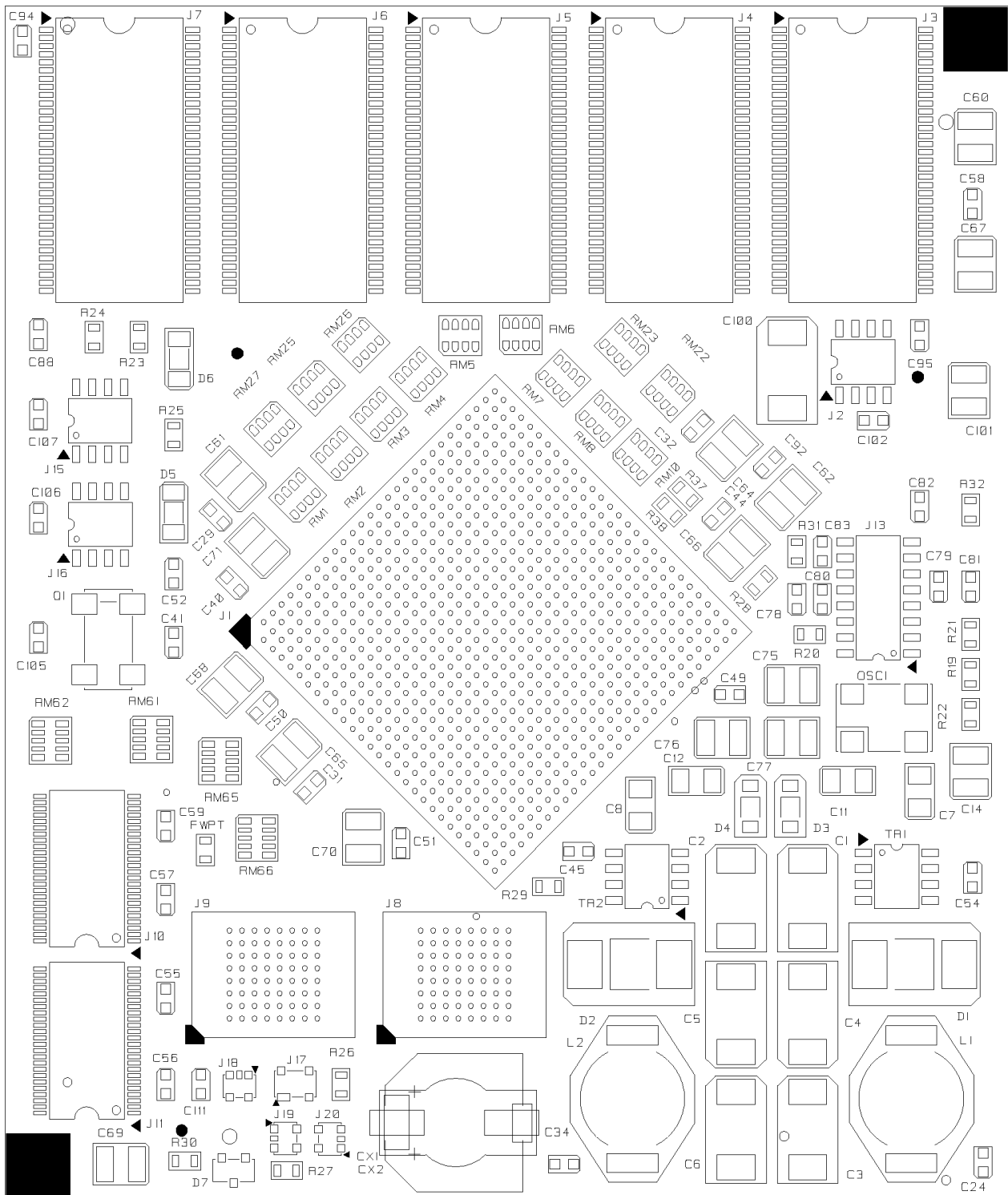
Pin	Signal	Signal	Pin
79	PB23	PD14	80
81	PB24	PD15	82
83	PB25	PD16	84
85	PB26	PD17	86
87	PB27	PD18	88
89	PB28	PD19	90
91	PB29	PD20	92
93	PB30	PD21	94
95	PB31	PD22	96
97	PD25	PD23	98
99	PD24	ground	100

Appendices

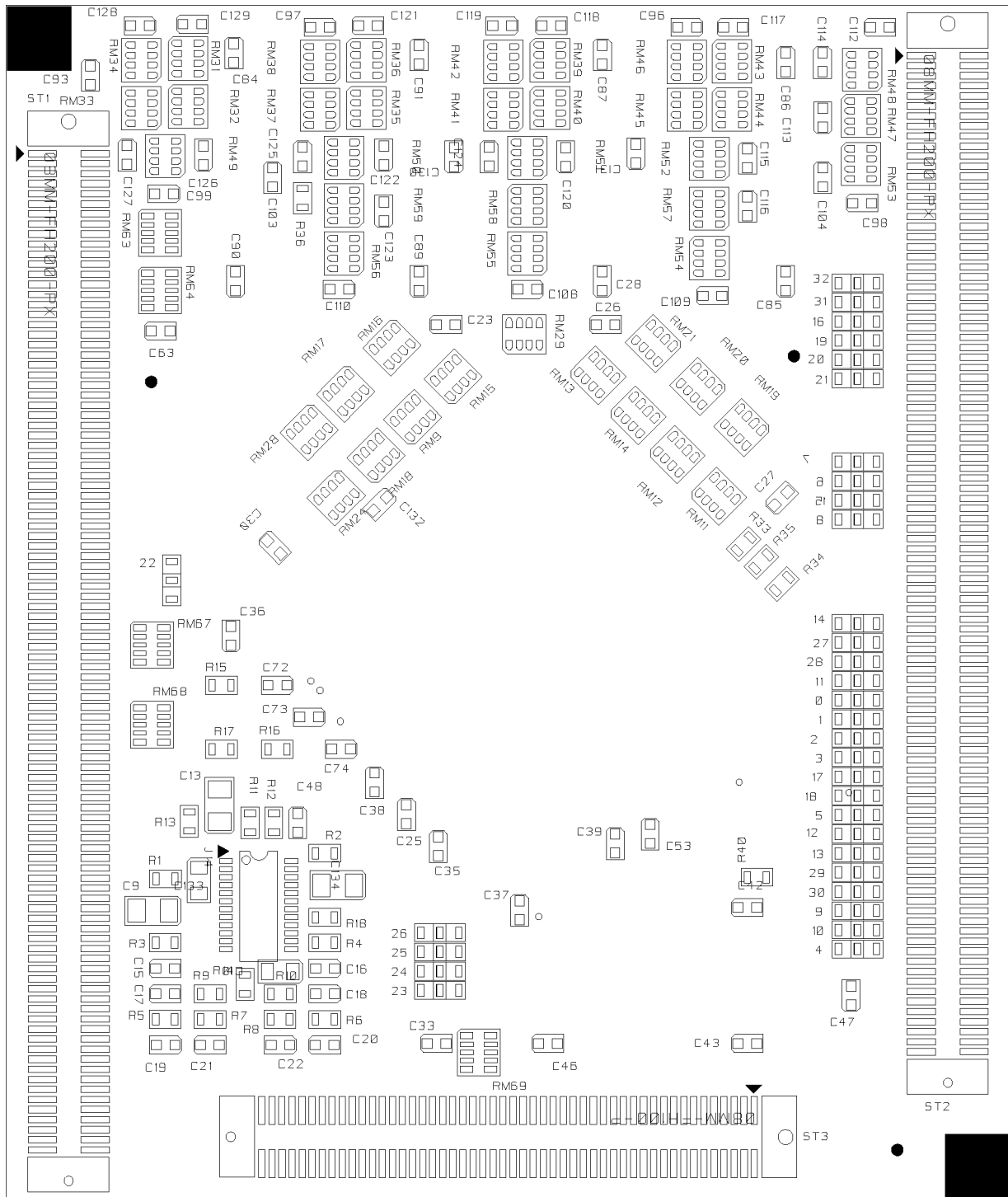
Appendix A: Factory default Link Setting



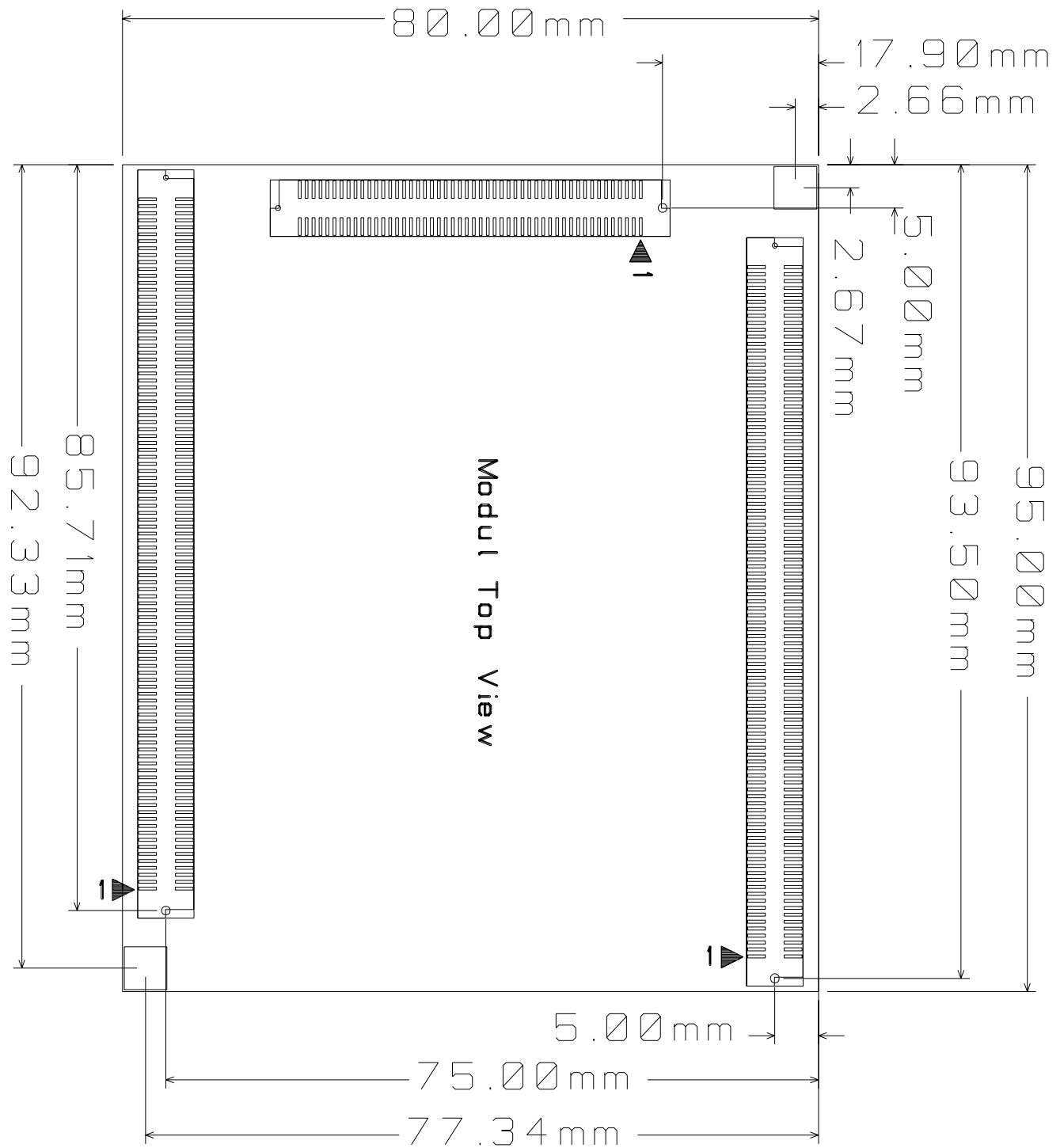
Appendix B: Layout Component Side



Appendix C: Layout Solder Side



Appendix D: Physical Dimensions (Bottom View)



All dimensions are given in millimeters

Physical Dimensions continued

The used connectors on the PM854 are 200 pin receptacles with 0,8mm pitch.
On PM856 an additional 100-pin receptacle is used for ST3.

200 pins (ST1, ST2) : e.g. AMP 177983-0 series

100 pins (ST3): e.g. AMP 177983-4 series

For carrier boards the mating plugs are necessary.

200 pins:

AMP 177984-0 series for 5 mm Board to Board distance

AMP 179029-0 series for 6 mm Board to Board distance

AMP 179030-0 series for 7 mm Board to Board distance

AMP 179031-0 series for 8 mm Board to Board distance

100 pins:

AMP 177984-4 series for 5 mm Board to Board distance

AMP 179029-4 series for 6 mm Board to Board distance

AMP 179030-4 series for 7 mm Board to Board distance

AMP 179031-4 series for 8 mm Board to Board distance

Maximum component height:

Solder side:	2,0 mm
Component side including 2mm PCB:	5.5 mm
Component side including 2mm PCB and Heat sink:	21.5 mm

Appendix E: Schematics PM854 (please contact *MicroSys*)