

Microsys

User's Manual

***miriac*[™] Power Module**

PM520 Rev. 1

2nd edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
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Germany

declare that the product

PM520

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89 / 336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73 / 23 EEC**.

Date:

Signature:

Position: General Manager

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Edition

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Table of Contents

1.	Introduction	6
1.1	Short Description	6
1.2	Specifications	7
1.3	Related Documentation	7
2.	Delivery	8
2.1	Items shipped with this unit	8
2.2	Hints for unpacking, handling and storing	8
3.	Installation	9
3.1	Items required for PM520 installation	9
3.2	Points to be observed	9
4.	Board Overview	10
4.1	Features PM520	10
5.	Addressmap PM520	11
6.	Functional Description	12
6.1	The MPC5200 Processor	12
6.2	Clock Configuration	12
6.2.1	The Boot Mode Configuration	13
6.2.2	The Reset Configuration Links	14
6.2.3	The JTAG / COP interface	15
6.3	Memory	16
6.3.1	The DRAM Area	16
6.3.2	The Flash Memory	17
6.3.3	Boot Options	18
6.4	The I ² C Bus	19
6.4.1	The EEPROM	19
6.4.2	The Real Time Clock	19
6.5	Miscellaneous	20
6.5.1	The Backup Feature	20
6.5.2	The Board Reset Function	20
6.5.3	Hardware Watchdog Timer	20
6.6	The PM520 Interrupt Structure	21
6.7	The MPC5200 functional Pin Usage	22
6.8	The Board Connectors	25
6.8.1	Pin Assignment of the Connector ST1	25
6.8.2	Pin Assignment of the Connector ST2	27
7.	Summary of Jumpers	29
	Appendices	30
	Appendix A: Layout Component Side	31
	Appendix B: Layout Solder Side	32
	Appendix C: Physical Dimensions (Top View)	33
	Appendix D: Schematics PM520 (in printed Manuals only)	35

1. Introduction

1.1 Short Description

The **miriac™ Power Module PM520** is powered by the Motorola PowerPC **MPC5200**.

It features a **32 bit** wide data bus for the **64 MByte SDR- or DDR-SDRAM** area and the **4 MByte Flash** memory bank..

The local **I²C**-Interface of the **MPC5200** controls a **2KByte EEPROM** and a **RTC** with backup feature.

The **PM520** offers all features of the **MPC5200** via external connections, like another **I²C**-port, **two MSCAN**-controllers, a **PCI** and a **ATA** bus interface, **six serial I/O** controllers, a **10/100MB Ethernet MAC**, an **USB 1.1** host port, a **SPI**-interface and an **IR** data port.

The complete **PCI / ATA / SRAM bus** as well as all **64 I/O lines** of the **MPC5200** are accessible by the carrier board through two 140 pin connectors.

The board is implemented in **CMOS technology**, which allows for a power consumption as low as: **3.3V / 2,1W @ 400 MHz** CPU speed.

1.2 Specifications

The power requirements for the PM520 board are shown in the following table.

Power Requirements:

+3.3V, +5% / -2.5%,	650 mA (typ. @400 MHz)
---------------------	------------------------

Environmental Requirements:

Operating Temperature	0 ° C to +70 ° C -40°C to +85°C optional
Relative Humidity	0 to 95 % (non-condensing)
Storage Temperature	-40 ° C to + 85 ° C

1.3 Related Documentation

The following manuals are applicable to the PM520:

- MPC5200 Microprocessor User’s Manual
- SDR-SDRAM Data Sheet
- DDR-SDRAM Data Sheet
- RC28FXXXJ3 Intel Strata Flash Memory Data Sheet
- PCF8563 Real-Time-Clock User’s Manual
- X24C164 EEPROM Data Sheet

2. Delivery

2.1 Items shipped with this unit

- User's Manual PM520 Hardware
- *MicroSys* shipping carton



ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or *MicroSys* shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moist free, dust free environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for PM520 installation

For installation of the PM520, the following items are required.

- Carrier board (e.g. CR825)
- Adequate rated power supply

3.2 Points to be observed

Before the unit is mounted onto the carrier, the following points should be observed.

- Unit requires +3.3V (+ 5 %, - 2,5 %).
- Check default jumper setting.



The operating temperature must never exceed it's specified range.

**GUARANTEE IS VOID IF UNIT IS OPERATED
OUT OF IT'S SPECIFICATIONS!**

4. Board Overview

4.1 Features PM520

Board Format:	87mm x 65mm (3.42inch x 2.56inch)
Main Processor:	MPC5200 with PowerPC 603e 32 Bit Memory Bus 32 Bit ATA / IDE / ROM / PCI bus 16 Kbyte instruction cache 16 Kbyte data cache instruction and data MMU double precision FPU up to 6 serial PSC channels Dual USB / CAN / I ² C Controller 10 / 100 BaseT Ethernet Interface digital BDLC-D Interface 8 General Purpose Timers SPI Controller IrDA interface
Dynamic RAM:	two SDR or DDR SDRAM devices 64 MByte capacity (up to 128 Mbyte optional) 32 bit data bus width
Flash Memory:	8 MByte capacity (up to 64 Mbyte optional) 32 bit data bus width single 3.3 volt programmable devices
EEPROM:	I ² C serial access device 2KByte capacity
Real Time Clock:	I ² C serial access device PCF8563 with time & date function backup function with onboard gold cap
Data backup:	short time backup via service free gold cap external backup via standby line
Watchdog:	hardware watchdog timer with system reset
Power Supply:	single 3.3V board supply onboard dual 2 phase step down controller 1.8V core voltage supply 2.5V DDR SDRAM supply

5. Address map PM520

Type	Base	End	Select	Bus	Size
SDRAM Bank	0x0000 0000	Dram Size	MCS0		32Bit
Flash Memory Bank (8 MB)	0xFF80 0000	0xFFFF FFFF	CS0		32Bit
			CS1		8Bit
			CS2		
			CS3		
			CS4		
			CS5		
Watchdog Enable & Trigger Port			external		

Note!

The Address map given is *MicroSys* default.

All CS areas are programmable, so it may vary with different operating systems.

Type	write	read	
24C164 EEPROM	\$B0..\$BE	\$B1..\$BF	I ² C-Bus
PCF8563 Real Time Clock	\$A2	\$A3	I ² C-Bus

6. Functional Description

6.1 The MPC5200 Processor

The PM520 uses the MPC5200 RISC microprocessor from Motorola. It can be configured for different CPU core and bus speed versions. The MPC5200 contains a 603e compatible core with a 16 Kbyte data cache, a 16 Kbyte instruction cache, a data and instruction MMU and a double precision FPU. It uses a 3.3V bus supply, a 1.8V core supply voltage and, if mounted, a 2.5V DDR SDRAM interface supply. The local flash memory is connected in multiplexed 32 bit mode. The processor works with CPU clock rates up to 400MHz and a system bus clock rate up to 133MHz. The PM520 uses a fixed system clock input frequency of 33MHz. The reset configuration word can be adjusted via 2 x 16 soldering links.

6.2 Clock Configuration

SYS-XTAL-IN: **33MHz**

CFG 7: **0 = x1**
 1 = x2

CFG 6: **0 = x16**
 1 = x12

CFG 5: **0 = / 4**
 1 = / 8

PPC-PLL-CFG(0:4): **00010**

IPB-CLK-SEL: 0 = / 1
 1 = / 2

PCI-CLK-SEL: 0 = / 1
 1 = / 2
 2 = / 4

33MHz *CFG7 * CFG6 / CFG5 = Memory-Clock = **132MHz**

Memory-Clock * PPC-PLL-CFG = Core-Clock = **396MHz**

Memory-Clock / IPB-CLK-SEL = IPB-Clock = **66MHz**

IPB-Clock / PCI-CLK-SEL = PCI-Clock = **33MHz**

6.2.1 The Boot Mode Configuration

The PM520 can work with an 8 or 32 bit boot ROM. The 32 bit setting is used for onboard flash, while the 8 bit mode can only be used via an external 8 bit boot device, connected to the appropriate lines of the ST1 connector via the carrier board.

The 32 bit or 8 bit boot mode via CS0 can be configured by jumper BTMD.

BTMD	Function
Pin 1-2	CS0 connected to external 8 bit device CS1 connected to local 32bit Flash
Pin 3-4 (default)	CS0 connected to local 32bit Flash CS1 connected to external 8 bit device

6.2.2 The Reset Configuration Links

The PM520 contains 2 x 16 links for a functional power up configuration of the MPC5200 processor according to following table. The links on the CFL side will set the config line to low while the links on the CFH side will pull them up, i.e. only one link of a CFL / CFH group must be installed at a time.

CFL / CFH	Processor Signal	Function	Description
0	ATA-DACK	PPC-PLL-CFG-4	Core PLL Configuration Bit 4
1	ATA-IOR	PPC-PLL-CFG-3	Core PLL Configuration Bit 3
2	ATA-IOW	PPC-PLL-CFG-2	Core PLL Configuration Bit 2
3	LP-RWB	PPC-PLL-CFG-1	Core PLL Configuration Bit 1
4	LP-ALE	PPC-PLL-CFG-0	Core PLL Configuration Bit 0
5	LP-TS	XLB-CLK-SEL	XLB Clock Divider (0 = 4, 1 = 8)
6	USB1-1	SYS-PLL-CFG-0	SYS PLL Divider (0 = 16, 1 = 12)
7	USB1-2	SYS-PLL-CFG-1	SYS PLL Divider (0 = 1, 1 = 2)
8	ETH-0	BOOT-ROM-MG	Boot / No-Boot in Most Graphic Mode
9	ETH-1	LARGE-FLASH-SEL	Boot / No-Boot in Large Flash Mode
10	ETH-2	PPC-MSRIP	PPC Boot Address / Exception Table
11	ETH-3	BOOT-ROM-WAIT	IPB-Waitstates (0 = 4, 1 = 48)
12	ETH-4	BOOT-ROM-SWAP	Byte Lane Swap (0 = no, 1 = yes)
13	ETH-5	BOOT-ROM-SIZE	0 = 8 bit non muxed, 1 = 32bit muxed
14	ETH-6	BOOT-ROM-TYPE	0 = non muxed, 1 = muxed
15	ETH-7	PPC-TLE	1 = PPC true little endian

If the multiplexer J16 and BTMD jumper field are installed, the reset configuration links 13 and 14 must not be populated on either side, because the boot device configuration is automatically done by an onboard circuitry.

6.2.3 The JTAG / COP interface

The **JTAG / COP** interface of the PM520 can only be used via the carrier board. The 140 pin SMD connector ST1 contains the necessary lines according to the following table.

ST1	Signal
Pin 1	GND
Pin 3	TMS
Pin 5	TCK
Pin 7	TRST#
Pin 9	TDO
Pin 11	TDI
Pin 107	GND
Pin 115	CKSTPO#
Pin 117	SRST#
Pin 119	HRST#

6.3 Memory

6.3.1 The DRAM Area

The PM520 can be fitted out either with two single or two **Double Data Rate Synchronous Dynamic RAM** devices which allows for a total capacity from 16MByte to 128MByte, depending on the used chip sizes. The ram bank is directly controlled by the MCS0 select line of the MPC5200. The SDRAM data port is 32 bits wide.



For detailed information about the SDRAM chip specification, please refer to the according SDRAM data sheet.

6.3.2 The Flash Memory

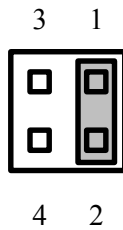
The flash memory area of the PM520 consists of two devices with a total capacity 8Mbyte. The 32 bit wide flash bank can be controlled via the CS0 or the CS1 line on the **LocalPlus** bus of the MPC5200. The selection and power up configuration between both CS-lines is performed via jumper BTMD. If the link is set to BTMD(3-4), the local flash memory is connected to the CS0 line, while the CS1 line of the MPC5200 is configured for an external 8 bit non multiplexed mode device. The WAIT pins of both local flash devices are not connected and left floating. The ADV pin is connected to the CE line, in case of special burst Flashes are used. The VPEN pins of both devices are tied to high.



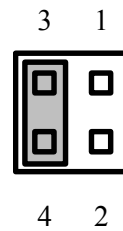
**For detailed chip information see Technical manual
of Intel 28FXXXJ3 Strata Flash**

6.3.3 Boot Options

The PM520 can be configured to boot either from an external 8Bit device, or from the local 32Bit Flash ROM bank after Reset. The selection is done by jumper BTMD. When set to 3-4, the factory default setting, the MPC5200 boots from the local 32Bit flash. If BTMD is set to 1-2, the MPC5200 boots from an external 8bit device.



Boot from external 8 Bit device.



Boot from local 32Bit Flash (default).

6.4 The I²C Bus

The local I²C bus onboard the PM520 is driven via the I2C1-IO and the I2C1-CLK pins of the MPC5200 and controls the real-time clock and an EEPROM device. The second I²C bus of the MPC5200 is not used onboard.

6.4.1 The EEPROM

The PM520 offers a 16KBit serial EEPROM for storing system or board parameters. The X24C164 device is internally organized to 2048 x 8 bit and allows for at least 100000 write cycles with a typical cycle time of 5ms.

The 24C164 device responds on the I²C bus at address \$B1 for read and \$B0 for write accesses.



**For detailed programming information and chip description,
please refer to X24C164 Data Sheet !**

6.4.2 The Real Time Clock

The PCF8563 RTC features a clock function with a calendar and an universal timer with alarm and interrupt function. The RTC is protected against data loss by a backup circuitry. The backup feature supplied from a service free gold capacitor cannot be disabled. For long time applications the standby line on **ST1 pin 109** can be used to supply the necessary backup power. The low active RTC interrupt signal is connected on the MPC5200 IRQ line 2, if R13 is installed (default).

The RTC device responds to the I²C bus at address \$A3 for read and \$A2 for write accesses.



**For detailed programming information and chip description,
please refer to Philips PCF8563 Data Sheet !**

6.5 Miscellaneous

6.5.1 The Backup Feature

The backup feature of the PM520 is used to protect the **RTC**. The backup power is supplied by a **service free gold capacitor** as well as by a standby line of connector ST1. The RTC cannot be disconnected from the backup power.

The gold capacitor allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended the backup power can be supplied via the standby line on connector ST1, pin 109. The external supply voltage should not exceed 3,6 volts and not fall below 2.5 volts to ensure correct data retention.

6.5.2 The Board Reset Function

During power up or power down sequences, the board supervisory circuits MAX-823 and MAX-811 activates the board reset line and holds the PM520 in a defined state. The reset line will be low for at least 250ms if the supply voltage reaches 3.0 volts. Below that voltage, the reset line will be continuously low.

6.5.3 Hardware Watchdog Timer

The PM520 features a fixed rate hardware timer for watchdog purposes (MAX823), which can be enabled by software. Once enabled by an access to signal CSWDG, it only can be disabled by a hardware reset. The time out rate is set to 1.6 seconds by default. Within that time at least one access must be performed to signal CSWDG, to retrigger the timer. The signal **CSWDG** leads to connector **ST1, Pin 98** and must be connected to a software controllable signal.

6.6 The PM520 Interrupt Structure

There are four low active interrupt lines onboard the PM520. The interrupt levels are used according to following table.

Level	MPC5200	External Source
0	IRQ0	not used, ST1 pin110
1	IRQ1	not used, ST1 pin112
2	IRQ2	Real Time Clock & ST1 pin114
3	IRQ3	not used, ST1 pin116

6.7 The MPC5200 functional Pin Usage

Signal	Pin	Functions	Usage
MA(0-12)	xxx	MA0 – MA12	SDRAM
MDQ(0-31)	xxx	MDQ0 – MDQ31	SDRAM
DQM(0-3)#	xxx	DQM-0 – DQM-3	SDRAM
MDQS(0-3)#	xxx	MDQS-0 – MDQS-3	SDRAM
MCS0#	B18	MCS0	SDRAM
MCAS#	B19	MCAS	SDRAM
MRAS#	A18	MRAS	SDRAM
MWE#	A19	MWE	SDRAM
MCKE	F20	MCKE	SDRAM
MCLK	G19	MCLK	SDRAM
MCLK#	G20	MCLK	SDRAM
MBA1	A17	MBA1	SDRAM
MBA0	C18	MBA0	SDRAM
AD(0-15)	xxx	AD0 – AD15 / A0 – A15 / D0 – D15	Flash / ST1-xxx
AD(16-23)	xxx	AD16 – AD23 / A16 – A23 / D16 – D23 / D0 – D7	Flash / ST1-xxx
AD(24-31)	xxx	AD24 – AD31 / A24 – A31 / D24 – D31 / D8 – D15 / D0 – D7	ST1-xxx
CS8R# / CS32R#	W14	CS-0	Boot-Flash / ST1-91
CS32R# / CS8R#	Y14	CS-1	Flash / ST1-92
CS2#	V15	CS-2	non / ST1-93
CS3#	W15	CS-3	non / ST1-94
CS4#	Y15	CS4 / ATA-CS0	non / ST1-95
CS5#	V16	CS5 / ATA-CS1	non / ST1-96
LP-TS#	Y13	LP-TS	non / ST1-83
LP-ACK#	U14	LP-ACK	non / ST1-85
LP-WE#	W16	LP-WE	non / ST1-86
LP-ALE#	V14	LP-ALE	non / ST1-87
LP-OE#	D8	LP-OE	non / ST1-88
ATA-DRQ	V17	ATA-DRQ	non / ST1-100
ATA-IOCHRDY	W18	ATA-IOCHRDY	non / ST1-101
ATA-DACK#	Y18	ATA-DACK	non / ST1-102
ATA-INTRQ	Y19	ATA-INTRQ	non / ST1-103
ATA-IOR#	Y17	ATA-IOR	non / ST1-104
ATA-ISOLATE	Y16	ATA-ISOLATE	non / ST1-105
ATA-IOW#	W17	ATA-IOW	non / ST1-106
I2C2-CLK	V20	I2C2-CLK / ATA-CS0	local I ² C
I2C2-IO	W20	I2C2-IO / ATA-CS1	local I ² C
CAN1-TX	V19	I2C1-CLK / CAN1-TX	ST2-41
CAN1-RX	W19	I2C1-IO / CAN1-RX	ST2-39

The MPC5200 functional Pin Usage continued:

Signal	Pin	Functions	Usage
CLK	T1	PCI-CLK / CLK-OUT	non / ST1-4
RST#	R2	PCI-RESET / A15	non / ST1-16
CBE0#	W10	PCI-CBE0 / A1 / A17	non / ST1-73
CBE1#	Y8	PCI-CBE1 / A2 / A18	non / ST1-74
CBE2#	W6	PCI-CBE2 / A3 / A19	non / ST1-37
CBE3#	Y2	PCI-CBE3 / A4 / A20	non / ST1-38
GNT#	R4	PCI-GNT / A14	non / ST1-41
REQ#	U1	PCI-REQ / A13	non / ST1-43
SERR#	W8	PCI-SERR / A10	non / ST1-44
PERR#	Y7	PCI-PERR / A11	non / ST1-45
IDSEL	U2	PCI-IDSEL / A12	non / ST1-46
DVSEL#	W7	PCI-DEVSEL / A8 / A24	non / ST1-47
STOP#	V6	PCI-STOP / A7 / A23	non / ST1-48
IRDY#	Y6	PCI-IRDY / A6 / A22	non / ST1-49
TRDY#	W5	PCI-TRDY / A5 / A21	non / ST1-50
FRAME#	V5	PCI-FRAME / A9 / A25	non / ST1-51
PAR	V7	PCI-PAR / A0 / A16	non / ST1-52

Signal	Pin	Functions	Usage
IR-RX	B12	GPIO-WKUP4 / IR-RX	non / ST2-128
IRDA-RX	C11	GPIO-WKUP5 / IRDA-RX	non / ST2-132
GPIO-WKUP6	C15	GPIO-WKUP6	non / ST2-86
GPIO-WKUP7	C12	GPIO-WKUP7	non / ST2-88
IR-TX	A12	GPIO-IRDA0 / IRDA-TX / IR-TX	non / ST2-134
IR-USB-CLK	C13	GPIO-IRDA1 / IR-USB-CLK	non / ST2-136
TIMER-0	Y20	GPIO-TIMER0 / ATA-CS0 / CAN2-TX	non / ST2-25
TIMER-1	V18	GPIO-TIMER1 / ATA-CS1 / CAN2-RX	non / ST2-23
TIMER-2	D3	GPIO-TIMER2 / SPI-MOSI	non / ST2-12
TIMER-3	D2	GPIO-TIMER3 / SPI-MISO	non / ST2-14
TIMER-4	D1	GPIO-TIMER4 / SPI-SS	non / ST2-16
TIMER-5	E3	GPIO-TIMER5 / SPI-CLK	non / ST2-20
TIMER-6	E2	GPIO-TIMER6	non / ST2-22
TIMER-7	E1	GPIO-TIMER7	non / ST2-24

The MPC5200 functional Pin Usage continued:

Signal	Pin	Functions	Usage
PSC1-0	B11	GPIO-PSC1-0 / UART1-TXD / CODEC1-TXD / AC97-1-SDATA-OUT	non / ST2-10
PSC1-1	A11	GPIO-PSC1-1 / UART1-RXD / CODEC1-RXD / AC97-1-SDATA-IN	non / ST2-3
PSC1-2	C10	GPIO-PSC1-2 / UART1-RTS / AC97-1-SYNC	non / ST2-7
PSC1-3	B10	GPIO-PSC1-3 / UART1-CTS / CODEC1-CLK / AC97-1-BITCLK	non / ST2-73
PSC1-4	A10	GPIO-WKUP0 / PSC1-4 / UART1-CD / CODEC1-FRAME / AC97-1-RES	non / ST2-105
PSC2-0	C9	GPIO-PSC2-0 / UART2-TXD / CODEC2-TXD / AC97-2-SDATA-OUT / CAN1-TXD	non / ST2-11
PSC2-1	B9	GPIO-PSC2-1 / UART2-RXD / CODEC2-RXD / AC97-2-SDATA-IN / CAN1-RXD	non / ST2-40
PSC2-2	A9	GPIO-PSC2-2 / UART2-RTS / AC97-2-SYNC / CAN2-TXD	non / ST2-13
PSC2-3	B8	GPIO-PSC2-3 / UART2-CTS / CODEC2-CLK / AC97-2-BITCLK / CAN2-RXD	non / ST2-75
PSC2-4	A8	GPIO-WKUP1 / PSC2-4 / UART2-CD / CODEC2-FRAME / AC97-2-RES	non / ST2-111
PSC3-0	C7	GPIO-PSC3-0 / UART3-TXD / CODEC3-TXD / USB2-OE	non / ST2-56
PSC3-1	B7	GPIO-PSC3-1 / UART3-RXD / CODEC3-RXD / USB2-TXN	non / ST2-42
PSC3-2	A7	GPIO-PSC3-2 / UART3-RTS / CODEC3-CLK / USB2-TXP	non / ST2-21
PSC3-3	C6	GPIO-PSC3-3 / UART3-CTS / CODEC3-FRAME / USB2-RXD	non / ST2-113
PSC3-4	B6	GPIO-SINT0 / PSC3-4 / UART3-CD / USB2-RXP	non / ST2-115
PSC3-5	A6	GPIO-SINT1 / PSC3-5 / USB2-RXN	non / ST2-138
PSC3-6	C5	GPIO-PSC3-4 / PSC3-6 / SPI-MOSI / USB2-PORTPWR	non / ST2-33
PSC3-7	B5	GPIO-PSC3-5 / PSC3-7 / SPI-MISO / USB2-SPEED	non / ST2-29
PSC3-8	A5	GPIO-SINT2 / PSC3-8 / SPI-SS / USB2-SUSPEND	non / ST2-29
PSC3-9	C4	GPIO-WKUP2 / PSC3-9 / SPI-CLK / USB2-OVERCURRENT	non / ST2-31
USB1-0	H1	GPIO-USB0 / USB1-OE	non / ST2-110
USB1-1	H2	RST-CFG6 / USB1-TXN	non / ST2-112
USB1-2	H3	RST-CFG7 / USB1-TXP	non / ST2-114
USB1-3	G1	USB1-RXD	non / ST2-116
USB1-4	G2	USB1-RXP	non / ST2-118
USB1-5	G3	USB1-RXN	non / ST2-120
USB1-6	G4	GPIO-USB1 / USB1-PORTPWR	non / ST2-122
USB1-7	F1	GPIO-USB2 / USB1-SPEED	non / ST2-124
USB1-8	F2	GPIO-USB3 / USB1-SUSPEND	non / ST2-123
USB1-9	F3	GPIO-SINT3 / USB1-OVERCURRENT	non / ST2-121
ETH-0	K1	RST-CFG8 / GPIO-ETH0 / ETH-TTXEN	non / ST2-76
ETH-1	K2	RST-CFG9 / GPIO-ETH1 / ETH-TXD0	non / ST2-98
ETH-2	K3	RST-CFG10 / GPIO-ETH2 / ETH-TXD1 / USB2-TXP	non / ST2-96
ETH-3	J1	RST-CFG11 / GPIO-ETH3 / ETH-TXD2 / USB2-PORTPWR	non / ST2-94
ETH-4	J2	RST-CFG12 / GPIO-ETH4 / ETH-TXD3 / USB2-SPEED	non / ST2-92
ETH-5	L3	RST-CFG13 / GPIO-ETH5 / ETH-TXERR / USB2-SUSPEND	non / ST2-74
ETH-6	N2	RST-CFG14 / GPIO-ETH6 / ETH-USB2-OE	non / ST2-85
ETH-7	N1	RST-CFG15 / GPIO-ETH7 / ETH-USB2TXN	non / ST2-83
ETH-8	M3	GPIO-ETH10 / ETH-RXDV-CD	non / ST2-78
ETH-9	L1	GPIO-ETH11 / ETH-RXCLK	non / ST2-91
ETH-10	J3	GPIO-ETH12 / ETH-COL	non / ST2-68
ETH-11	L4	GPIO-ETH13 / ETH-TXCLK	non / ST2-87
ETH-12	M2	ETH-RXD0	non / ST2-100
ETH-13	M1	GPIO-SINT4 / ETH-RXD1 / USB2-RXD	non / ST2-102
ETH-14	N4	GPIO-SINT5 / ETH-RXD2 / USB2-RXP	non / ST2-104
ETH-15	N3	GPIO-SINT6 / ETH-RXD3 / USB2-RXN	non / ST2-106
ETH-16	L2	GPIO-SINT7 / ETH-RXERR / USB2-OVERCURRENT	non / ST2-80
ETH-17	J4	GPIO-WKUP3 / ETH-CRS	non / ST2-70

6.8 The Board Connectors

The PM520 uses two 140 pin connectors to link all power, bus and communication lines to the carrier board.

6.8.1 Pin Assignment of the Connector ST1

Pin	Signal	Signal	Pin
1	ground	ground	2
3	JTMS	CLK	4
5	JTCK		6
7	JTRST#		8
9	JTDO		10
11	JTDI		12
13	CLK (conn. to pin 4)		14
15		A15 / RST#	16
17	ground	ground	18
19	AD30	AD31	20
21	AD28	AD29	22
23	AD26	AD27	24
25	AD24	AD25	26
27	AD22	AD23	28
29	AD20	AD21	30
31	AD18	AD19	32
33	AD16	AD17	34
35	ground	ground	36
37	A3 / A19 / CBE2#	A4 / A20 / CBE3#	38
39			40
41	A14 / GNT#		42
43	A13 / REQ#	A10 / SERR#	44
45	A11 / PERR#	A12 / IDSEL	46
47	A8 / A24 / DVSEL#	A7 / A23 / STOP#	48
49	A6 / A22 / IRDY#	A5 / A21 / TRDY#	50
51	A9 / A25 / FRAME#	A0 / A16 / PAR	52
53	ground	ground	54
55	AD14	AD15	56
57	AD12	AD13	58
59	AD10	AD11	60
61	AD8	AD9	62
63	AD6	AD7	64
65	AD4	AD5	66
67	AD2	AD3	68
69	AD0	AD1	70

pin assignment of the connector ST1 continued

Pin	Signal	Signal	Pin
71	ground	ground	72
73	A1 / A17 / CBE0#	A2 / A18 / CBE1#	74
75			76
77			78
79			80
81			82
83	LP-TS#		84
85	LP-ACK#	LP-WE#	86
87	LP-ALE#	LP-OE#	88
89	ground	ground	90
91	CS8R#	CS32R#	92
93	CS2#	CS3#	94
95	ATA-CS0 / CS4#	ATA-CS1 / CS5#	96
97		CSWDG#	98
99		A16 / ATA-DRQ	100
101	A20 / ATA-IOCHRDY	A17 / ATA-DACK	102
103	A21 / ATA-INTRQ	A18 / ATA-IOR#	104
105	A22 / ATA-ISOLATE	A19 / ATA-IOW#	106
107	ground	ground	108
109	STDBY	IRQ0#	110
111	KRST#	IRQ1#	112
113		IRQ2#	114
115	TEST-SEL0	IRQ3#	116
117	SRST#		118
119	HRST#		120
121	PORST#		122
123			124
125	ground	ground	126
127			128
129			130
131	VDD	VDD	132
133	VDD	VDD	134
135	VDD	VDD	136
137	VDD	VDD	138
139	ground	ground	140

6.8.2 Pin Assignment of the Connector ST2

Pin	Signal	Signal	Pin
1	ground	ground	2
3	GPIO-PSC1-1		4
5			6
7	GPIO-PSC1-2		8
9		GPIO-PSC1-0	10
11	GPIO-PSC2-0	GPIO-TIMER-2	12
13	GPIO-PSC2-2	GPIO-TIMER-3	14
15		GPIO-TIMER-4	16
17	ground	ground	18
19		GPIO-TIMER-5	20
21	GPIO-PSC3-2	GPIO-TIMER-6	22
23	GPIO-TIMER-1	GPIO-TIMER-7	24
25	GPIO-TIMER-0		26
27			28
29	GPIO-PSC3-8		30
31	GPIO-PSC3-9		32
33	GPIO-PSC3-6		34
35	ground	ground	36
37	GPIO-PSC3-7		38
39	I ² C2-IO / CAN-RX1	GPIO-PSC2-1	40
41	I ² C2-CLK / CAN-TX1	GPIO-PSC3-1	42
43			44
45			46
47			48
49			50
51			52
53	ground	ground	54
55		GPIO-PSC3-0	56
57			58
59			60
61			62
63			64
65			66
67		GPIO-ETH-10	68
69		GPIO-ETH-17	70

pin assignment of the connector ST2 continued

Pin	Signal	Signal	Pin
71	ground	ground	72
73	GPIO-PSC1-3	GPIO-ETH-5	74
75	GPIO-PSC2-3	GPIO-ETH-0	76
77		GPIO-ETH-8	78
79		GPIO-ETH-16	80
81			82
83	GPIO-ETH-7		84
85	GPIO-ETH-6	GPIO-WKUP6	86
87	GPIO-ETH-11	GPIO-WKUP7	88
89	ground	ground	90
91	GPIO-ETH-9	GPIO-ETH-4	92
93		GPIO-ETH-3	94
95		GPIO-ETH-2	96
97		GPIO-ETH-1	98
99		ETH-12	100
101		GPIO-ETH-13	102
103		GPIO-ETH-14	104
105	GPIO-PSC1-4	GPIO-ETH-15	106
107	ground	ground	108
109		GPIO-USB1-0	110
111	GPIO-PSC2-4	USB1-1	112
113	GPIO-PSC3-3	USB1-2	114
115	GPIO-PSC3-4	USB1-3	116
117		USB1-4	118
119		USB1-5	120
121	GPIO-USB1-9	GPIO-USB1-6	122
123	GPIO-USB1-8	GPIO-USB1-7	124
125	ground	ground	126
127		GPIO-IR-RX	128
129			130
131		GPIO-IRDA-RX	132
133		GPIO-IR-TX	134
135		GPIO-IR-USB-CLK	136
137		GPIO-PSC3-5	138
139	ground	ground	140

7. Summary of Jumpers

Described function is valid, when jumper is set or link is intact !

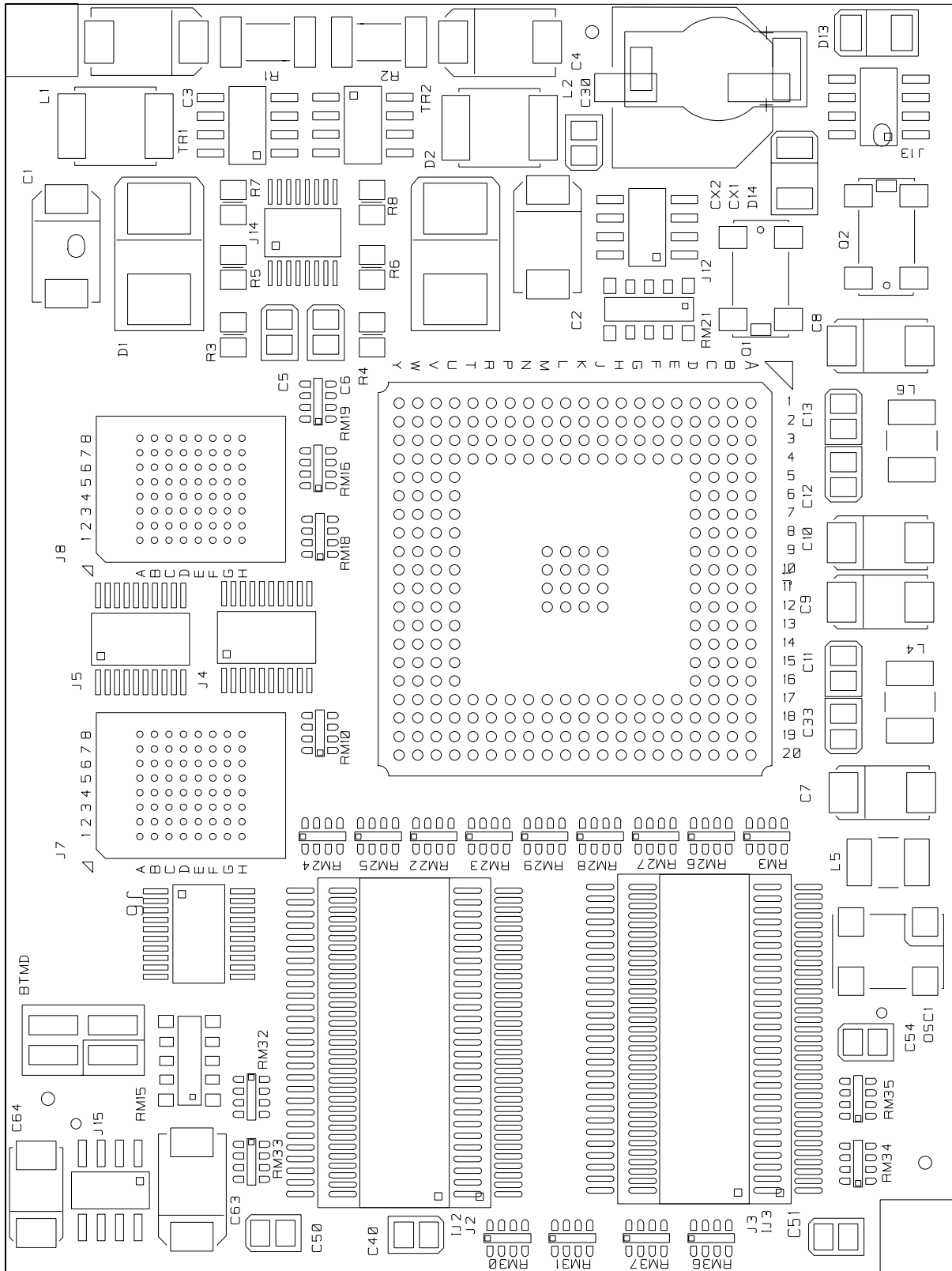
Size:	Name:	Default:	Position:	Function:
2x2	BTMD		1-2	CS0 – 8 bit device, CS1 – 32 bit flash
		#	3-4	CS0 – 32 bit flash, CS1 – 8 bit device
10x2	<i>CFx0-4</i>	<i>0, 1, 2, 4</i>	<i>CFL0-4</i>	<i>PPC-Core PLL low active bits</i>
		<i>3</i>	<i>CFH0-4</i>	<i>PPC-Core PLL high active bits</i>
2x2	<i>CFx5</i>	#	<i>CFL5</i>	<i>XLB-CLK = SYS-PLL FVCO / 4</i>
			<i>CFH5</i>	<i>XLB-CLK = SYS-PLL FVCO / 8</i>
2x2	<i>CFx6</i>	#	<i>CFL6</i>	<i>SYS-PLL FVCO = 16 x SYS-PLL-FREF</i>
			<i>CFH6</i>	<i>SYS-PLL FVCO = 12 x SYS-PLL-FREF</i>
2x2	<i>CFx7</i>	#	<i>CFL7</i>	<i>VCO = SYS-PLL-VCO</i>
			<i>CFH7</i>	<i>VCO = 2 x SYS-PLL-VCO</i>
2x2	<i>CFx8</i>	#	<i>CFL8</i>	<i>No Boot in Most Graphics Mode</i>
			<i>CFH8</i>	<i>Boot in Most Graphics Mode</i>
2x2	<i>CFx9</i>	#	<i>CFL9</i>	<i>No Boot in Large Flash Mode</i>
			<i>CFH9</i>	<i>Boot in Large Flash Mode</i>
2x2	<i>CFx10</i>		<i>CFL10</i>	<i>Boot Address / Exception Table \$0000 0100</i>
		#	<i>CFH10</i>	<i>Boot Address / Exception Table \$FFF0 0100</i>
2x2	<i>CFx11</i>		<i>CFL11</i>	<i>4 IP bus clocks of wait state</i>
		#	<i>CFH11</i>	<i>48 IP bus clocks of wait state</i>
2x2	<i>CFx12</i>	#	<i>CFL12</i>	<i>no byte lane swap, same endian ROM image</i>
			<i>CFH12</i>	<i>byte lane swap, different endian ROM image</i>
2x2	<i>CFx13</i>	<i>Note1</i>	<i>CFL13</i>	<i>8 bit non-muxed boot ROM</i>
			<i>CFH13</i>	<i>32 bit muxed boot ROM</i>
2x2	<i>CFx14</i>	<i>Note1</i>	<i>CFL14</i>	<i>non-muxed boot ROM bus</i>
			<i>CFH14</i>	<i>muxed boot ROM bus</i>
2x2	<i>CFx15</i>	#	<i>CFL15</i>	<i>not defined</i>
			<i>CFH15</i>	<i>Power PC True Little Endian</i>

Note 1: Links CFx13 and CFx14 must not be installed if Jumper field BTMD is available!

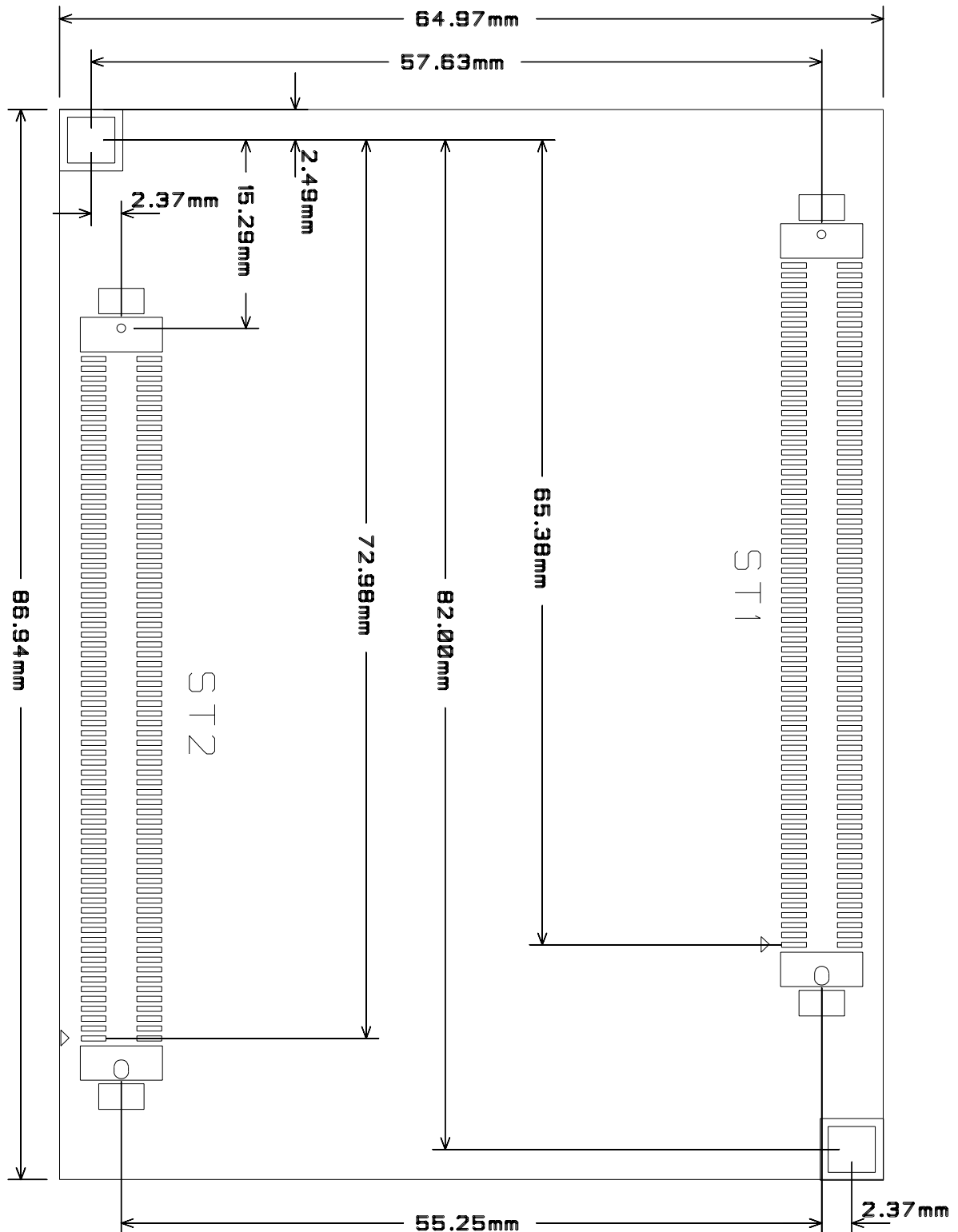
All Jumpers shown in *Italic* characters are solder inks!

Appendices

Appendix A: Layout Component Side



Appendix C: Physical Dimensions (Top View)



Physical Dimensions continued

The used connectors on the PM520 are 140 pin receptacles with 0,8mm pitch.

e.g. FCI 61082-14 or AMP 0177983-6 series

For carrier boards the mating plugs are necessary.

e.g. FCI 61083-14 or AMP 0177984-6 series for 5mm Board to Board distance

AMP 0179029-6 series for 6mm Board to Board distance

AMP 0179030-6 series for 7mm Board to Board distance

AMP 0179031-6 series for 8mm Board to Board distance

Maximum component height:

Solder side: 2.5mm

Component side including 2mm PCB: 7.5mm

Appendix D: Schematics PM520 (in printed Manuals only)