

# **Microsys**

**User's Manual**

**MPX8349 Rev. 3**

**1<sup>st</sup> edition**

# Declaration of Conformity

We, Manufacturer  
MicroSys Electronics GmbH  
Mühlweg 1  
D-82054 Sauerlach  
Germany

Declare that the product

**MPX8349**

is in conformity with:

**EN 50081-1 Generic Emission Standard**  
**EN 50082-1 Generic Immunity Standard**

in accordance with **89/336 EEC-EMC Directive**.

We also declare the conformity of the above-mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position:       General Manager

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## Edition

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## Table of Contents

1. Chip Select Overview.....	7
2. Address map.....	7
3. I <sup>2</sup> C Address Overview.....	7
4. Power Supply Ratings.....	8
5. Backup Supply Ratings.....	8
6. The MPC8349E Processor.....	9
7. BDM JTAG Port Connection.....	9
8. Interrupt Configuration.....	10
9. Local Bus.....	11
9.1. Local Bus Pin Configuration.....	11
9.2. Local Bus ST1-Connector Pinout.....	12
10. PCI Interface.....	13
10.1. PCI Bus Clock Configuration.....	13
10.2. PCI Bus IDSEL Configuration.....	13
10.3. PCI Bus ST1-Connector Pinout.....	13
10.4. PCI Bus ST1-Connector Pinout.....	14
11. MII Interface ST2-Connector Pinout.....	15
12. USB & UART Interface ST2-Connector Pin out:.....	16
DDR SDRAM Memory.....	17
12.1. Memory Bus Pin Configuration.....	17
12.2. Memory Bound CS0-BNDS.....	18
12.3. Chips Select Configuration CS0-CONFIG.....	19
12.4. DDR SDRAM Timing Configuration Timing-CFG-1.....	20
12.5. DDR SDRAM Timing Configuration Timing-CFG-2.....	21
12.6. DDR SDRAM Control Configuration DDR-SDRAM-CFG.....	22
12.7. DDR SDRAM Interval Configuration DDR-SDRAM-INTERVAL.....	23
12.8. DDR SDRAM Mode Configuration Register DDR-SDRAM-MODE.....	24
13. Flash Memory.....	25
13.1. Base Register BR0.....	25
13.2. Option Register OR0.....	26
14. SRAM.....	27
14.1. SRAM Pin Configuration.....	27
14.2. Base Register BR1.....	28
14.3. Option Register OR1.....	29
15. DiskOnChip.....	30
15.1. DiskOnChip Pin Configuration.....	30
15.2. Base Register BR2.....	31
15.3. Option Register OR2.....	32
16. I <sup>2</sup> C EEPROM.....	33
16.1. EEPROM I <sup>2</sup> C Access Address.....	33
17. Real Time Clock PCF8563T.....	33
17.1. RTC I <sup>2</sup> C Access Address.....	33
17.2. RTC Address Map.....	34
18. Data Retention.....	35
18.1. Capacitor Backup Time.....	35
19. Hardware Watchdog Timer.....	35

Appendices .....	36
Layout Component Side .....	37
Layout Solder Side .....	38
Physical Dimensions (Top View) .....	39
Schematics MPX8349 (please contact <i>MicroSys</i> ).....	40

## 1. Chip Select Overview

<b>Signal</b>	<b>Function</b>	<b>Bus width</b>	<b>Mode</b>	<b>Size</b>	<b>Description</b>
CS0	FLASH	16 Bit	GPCM	16 MByte	connected to ST1B 18
CS1	SRAM	16 Bit	GPCM	1 MByte	connected to ST1B 20
CS2	DiskOnChip	16 Bit	GPCM	1 MByte	connected to ST1B 22
CS3	not used onboard	---	---	---	connected to ST1B 24
CS4	not used onboard	---	---	---	connected to ST1B 26
CS5	not used onboard	---	---	---	connected to ST1B 28

## 2. Address map

<b>Type</b>	<b>Base</b>	<b>End</b>	<b>Select</b>	<b>Bus</b>	<b>Size</b>
IMMRBAR	\$E000 0000	\$E00F FFFF			
SDRAM	\$0000 0000	\$0FFF FFFF	MCS0	603	64Bit
Flash	\$FC00 0000	\$FCFF FFFF	CS0	Local	16Bit
SRAM	\$F000 0000	\$F00F FFFF	CS1	Local	16Bit
DiskOnChip	\$F100 0000	\$F10F FFFF	CS2	Local	16Bit
not initialized			CS3		
not initialized			CS4		
not initialized			CS5		

## 3. I<sup>2</sup>C Address Overview

<b>Device</b>	<b>Hex</b>	<b>binary I<sup>2</sup>C address</b>							<b>read/write</b>
PCF8563T	A2/A3	1	0	1	0	0	0	1	1/0
AT24C128	A6/A7	1	0	1	0	0	1	1	1/0

## 4. Power Supply Ratings

The MPX8349 module must be supplied with single 3.3V and all pins of the module are 3.3V tolerant only. There is a 12 pin wide VDD supply block on connector ST2-C and several GND pins distributed over connector ST1 and ST2. For a proper operation, all ground pins and all VDD pins should be connected to the carrier board.

<b>3.3V</b>	<b>ST2-C</b>	<b>ST2-C</b>	<b>3.3V</b>
VDD	pin c41	pin c42	VDD
VDD	pin c43	pin c44	VDD
VDD	pin c45	pin c46	VDD
VDD	pin c47	pin c48	VDD
VDD	pin c49	pin c50	VDD
VDD	pin c51	pin c52	VDD

<b>Name</b>	<b>Rating</b>	<b>Current</b>	<b>Tolerance</b>	<b>Ripple</b>
VDD	+3.3VDC	peak 3A	+/-5%	max.50mV

## 5. Backup Supply Ratings

The MPX8349 contains a real-time clock and a static ram device. The data contents of both devices can be saved during short power down periods by the onboard gold capacitor. For extended backup times an external power can be supplied via the STDBY line.

<b>3.3V</b>	<b>ST2-C</b>
STDBY	c39

<b>Name</b>	<b>Rating</b>	<b>Current</b>	<b>Tolerance</b>	<b>Ripple</b>
STDBY	+3.3VDC	max. 2uA	+/-10%	max.50mV

## 6. The MPC8349E Processor

The MPC8349E CPU is connected to a 64+8 bit wide DDR SDRAM with ECC memory protection. The local bus side handles the onboard Flash, SRAM, and the DiskOnChip device by the select lines LCS0, LCS1 and LCS2, i.e. LCS3, LCS4 and LCS5 can be used for other purposes. The control lines of the local bus and both PCI interfaces are tied to high by 10kOhm pull-up resistors.

## 7. BDM JTAG Port Connection

The JTAG port of the MPC8349E can be accessed via ST2-A by the following signals:

<b>Signal</b>	<b>ST2</b>	<b>ST2</b>	<b>Signal</b>	<b>Description</b>
TMS	pin a33	pin a34	CKSTI	via link CKSI to signal IRQ6#
TDI	pin a35	pin a36	CKSTO	via link CKSO to signal IRQ7#
TDO	pin a37			
TCK	pin a39	pin a40	HRST#	
TRST#	pin a41	pin a42	SRST#	

### ATTENTION!

**During normal operation, the TRST# signal must be connected to ground. (Refer to carrier board description)**

## 8. Interrupt Configuration

<b>MPC8349E Signal</b>	<b>Destination</b>	<b>onboard source</b>
IRQ0#	ST2-a43	---
IRQ1#	ST2-a45	---
IRQ2#	ST2-a47	---
IRQ3#	ST2-a44	DiskOnChip IRQ via link DOC
IRQ4#	ST2-a46	---
IRQ5#	ST2-a48	---
IRQ6#	ST2-a50	---
IRQ7#	ST2-a52	INTA of PCI A

## 9. Local Bus

The local bus of the MPX8349 is accessible via the connectors ST1-A and ST1-B. Besides the LCLK1 and LCLK2 signal, all local bus lines are connected, even if onboard devices use some of them.

### 9.1. Local Bus Pin Configuration

<b>MPC8349E Signal</b>	<b>Destination</b>	<b>onboard function</b>
LAD(31:0)	ST1-A	Address/Data Bus
LCS0	ST1-b18	Flash Chip Select
LCS1	ST1-b20	SRAM Chip Select
LCS2	ST1-b22	DiskOnChip Select
LCS3	ST1-b24	not used
LGPL0	ST1-b17	not used
LGPL1	ST1-b19	SRAM / DiskOnChip
LGPL2	ST1-b21	Flash / SRAM / DiskOnChip
LGPL3	ST1-b23	not used
LGPL4	ST1-b25	not used
LGPL5	ST1-b27	not used
LALE	ST1-b15	address latches
LBCTL	ST1-b30	not used
LWE0	ST1-b10	Flash / SRAM
LWE1	ST1-b12	SRAM
LWE2	ST1-b14	not used
LWE3	ST1-b16	not used
LDP0	ST1-b5	not used
LDP1	ST1-b7	not used
LDP2	ST1-b2	not used
LDP3	ST1-b4	not used
LCLKE	ST1-b29	not used
LCLK0	ST1-b31	not used
LCLK1	----	DiskOnChip
LCLK2	----	not used
LA27	ST1-b9	Flash / SRAM / DiskOnChip
LA28	ST1-b11	Flash / SRAM / DiskOnChip
LA29	ST1-b13	Flash / SRAM / DiskOnChip
LA30	ST1-b6	Flash / SRAM / DiskOnChip
LA31	ST1-b8	not used

## 9.2. Local Bus ST1-Connector Pinout

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

GND	a1	a2	LAD8
GND	a3	a4	LAD9
LAD0	a5	a6	LAD10
LAD1	a7	a8	LAD11
LAD2	a9	a10	LAD12
LAD3	a11	a12	LAD13
LAD4	a13	a14	LAD14
LAD5	a15	a16	LAD15
LAD6	a17	a18	GND
LAD7	a19	a20	GND
LAD16	a21	a22	LAD24
LAD17	a23	a24	LAD25
LAD18	a25	a26	LAD26
LAD19	a27	a28	LAD27
LAD20	a29	a30	LAD28
LAD21	a31	a32	LAD29
LAD22	a33	a34	LAD30
LAD23	a35	a36	LAD31
GND	a37	a38	not connected
GND	a39	a40	not connected
not connected	a41	a42	not connected
B-REQ0	a43	a44	B-GNT0
B-REQ1	a45	a46	B-GNT1
B-REQ2	a47	a48	B-GNT2
B-RST	a49	a50	GND
B-PCICLK	a51	a52	GND

LDP2	b2	b1	GND
LDP3	b4	b3	GND
LA30	b6	b5	LDP0
LA31	b8	b7	LDP1
LWE0	b10	b9	LA27
LWE1	b12	b11	LA28
LWE2	b14	b13	LA29
LWE3	b16	b15	LALE
LCS0	b18	b17	LGPL0
LCS1	b20	b19	LGPL1
LCS2	b22	b21	LGPL2
LCS3	b24	b23	LGPL3
LCS4	b26	b25	LGPL4
LCS5	b28	b27	LGPL5
LBCTL	b30	b29	LCLKE
GND	b32	b31	LCLK0
GND	b34	b33	not connected
not connected	b36	b35	not connected
A-INTA	b38	b37	A-M66EN
A-GNT0	b40	b39	A-REQ0
A-GNT1	b42	b41	A-REQ1
A-GNT2	b44	b43	A-REQ2
A-GNT3	b46	b45	A-REQ3
A-GNT4	b48	b47	A-REQ4
A-RST	b50	b49	GND
A-PCICLK	b52	b51	GND

## 10. PCI Interface

The MPX8349 offers a single 64bit PCI interface or two 32bit interfaces. PCI interface A is located on connector ST1-D, while PCI interface B uses connector ST1-C. The according clock and arbiter signals are located on the connectors ST1-A and ST1-B. Some PCI signals of the MPC8349E are not available as external connections.

### 10.1. PCI Bus Clock Configuration

<b>MPC8349E Signal</b>	<b>Destination</b>	<b>Function</b>
PCI-CLK-OUT0	ST2-b52	PCI-A
PCI-CLK-OUT1	not connected	not used
PCI-CLK-OUT2	not connected	not used
PCI-CLK-OUT3	not connected	not used
PCI-CLK-OUT4	ST2-a51	PCI-B
PCI-CLK-OUT5	not connected	not used
PCI-CLK-OUT6	not connected	not used
PCI-CLK-OUT7	not connected	not used

### 10.2. PCI Bus IDSEL Configuration

<b>MPC8349E Signal</b>	<b>Destination</b>	<b>Function</b>
A-IDSEL	---	connected to AD31 via R36

### 10.3. PCI Bus ST1-Connector Pinout

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

## 10.4. PCI Bus ST1-Connector Pinout

not connected	a38	a37	GND
not connected	a40	a39	GND
not connected	a42	a41	not connected
B-GNT0	a44	a43	B-REQ0
B-GNT1	a46	a45	B-REQ1
B-GNT2	a48	a47	B-REQ2
GND	a50	a49	B-RST
GND	a52	a51	B-PCICLK

A-INTA	b38	b37	A-M66EN
A-GNT0	b40	b39	A-REQ0
A-GNT1	b42	b41	A-REQ1
A-GNT2	b44	b43	A-REQ2
A-GNT3	b46	b45	A-REQ3
A-GNT4	b48	b47	A-REQ4
A-RST	b50	b49	GND
A-PCICLK	b52	b51	GND

B-AD8/A-AD40	c2	c1	GND
B-AD9/A-AD41	c4	c3	GND
B-AD10/A-AD42	c6	c5	B-AD0/A-AD32
B-AD11/A-AD43	c8	c7	B-AD1/A-AD33
B-AD12/A-AD44	c10	c9	B-AD2/A-AD34
B-AD13/A-AD45	c12	c11	B-AD3/A-AD35
B-AD14/A-AD46	c14	c13	B-AD4/A-AD36
B-AD15/A-AD47	c16	c15	B-AD5/A-AD37
GND	c18	c17	B-AD6/A-AD38
GND	c20	c19	B-AD7/A-AD39
B-CBE1/A-CBE5	c22	c21	B-CBE0/A-CBE4
B-DVSL	c24	c23	B-FRME
B-PERR/A-REQ64	c26	c25	B-IRDY
B-SERR/A-ACK64	c28	c27	B-TRDY
B-PAR/A-PAR64	c30	c29	B-STOP
B-CBE3/A-CBE7	c32	c31	B-CBE2/A-CBE6
B-AD24/A-AD56	c34	c33	GND
B-AD25/A-AD57	c36	c35	GND
B-AD26/A-AD58	c38	c37	B-AD16/A-AD48
B-AD27/A-AD59	c40	c39	B-AD17/A-AD49
B-AD28/A-AD60	c42	c41	B-AD18/A-AD50
B-AD29/A-AD61	c44	c43	B-AD19/A-AD51
B-AD30/A-AD62	c46	c45	B-AD20/A-AD52
B-AD31/A-AD63	c48	c47	B-AD21/A-AD53
GND	c50	c49	B-AD22/A-AD54
GND	c52	c51	B-AD23/A-AD55

A-AD8	d2	d1	GND
A-AD9	d4	d3	GND
A-AD10	d6	d5	A-AD0
A-AD11	d8	d7	A-AD1
A-AD12	d10	d9	A-AD2
A-AD13	d12	d11	A-AD3
A-AD14	d14	d13	A-AD4
A-AD15	d16	d15	A-AD5
GND	d18	d17	A-AD6
GND	d20	d19	A-AD7
A-CBE1	d22	d21	A-CBE0
A-DVSL	d24	d23	A-FRME
A-PERR	d26	d25	A-IRDY
A-SERR	d28	d27	A-TRDY
A-PAR	d30	d29	A-STOP
A-CBE3	d32	d31	A-CBE2
A-AD24	d34	d33	GND
A-AD25	d36	d35	GND
A-AD26	d38	d37	A-AD16
A-AD27	d40	d39	A-AD17
A-AD28	d42	d41	A-AD18
A-AD29	d44	d43	A-AD19
A-AD30	d46	d45	A-AD20
A-AD31	d48	d47	A-AD21
GND	d50	d49	A-AD22
GND	d52	d51	A-AD23

all shaded PCI signals are tied to HIGH by 10kOhm pull-up resistors.

## 11. MII Interface ST2-Connector Pinout

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

MII-GTXCKI	a2	a1	GND
MII1-TXEN	a4	a3	GND
MII1-TXD1	a6	a5	MII1-TXD0
MII1-TXD3	a8	a7	MII1-TXD2
MII1-RXD0	a10	a9	MII1-GXCK
MII1-RXD2	a12	a11	MII1-RXD1
MII1-RXCK	a14	a13	MII1-RXD3
MII1-CRS	a16	a15	MII1-RXDV
MII1-TXD5	a18	a17	MII1-TXD4
MII1-TXD6	a20	a19	MII1-TXD7
MII1-RXD7	a22	a21	MII1-TXER
MII1-RXD5	a24	a23	MII1-RXD6
MII1-RXER	a26	a25	MII1-RXD4
MII1-TXCK1	a28	a27	MII1-COL
GND	a30	a29	MII-MDCK
GND	a32	a31	MII-MDIO
CKSTI	a34	a33	JTMS
CKSTO	a36	a35	JTDI
KRST	a38	a37	JTDO
HRST	a40	a39	JTCK
SRST	a42	a41	JTRST
IRQ3	a44	a43	IRQ0
IRQ4	a46	a45	IRQ1
IRQ5	a48	a47	IRQ2
IRQ6	a50	a49	GND
IRQ7	a52	a51	GND

CCLK	b2	b1	GND
MII2-TXEN	b4	b3	GND
MII2-TXD1	b6	b5	MII2-TXD0
MII2-TXD3	b8	b7	MII2-TXD2
MII2-RXD0	b10	b9	MII2-GXCK
MII2-RXD2	b12	b11	MII2-RXD1
MII2-RXCK	b14	b13	MII2-RXD3
MII2-CRS	b16	b15	MII2-RXDV
MII2-TXD5	b18	b17	MII2-TXD4
MII2-TXD7	b20	b19	MII2-TXD6
MII2-RXD7	b22	b21	MII2-TXER
MII2-RXD5	b24	b23	MII2-RXD6
MII2-RXER	b26	b25	MII2-RXD4
MII2-TXCK	b28	b27	MII2-COL
GND	b30	b29	CFGE
GND	b32	b31	PRST
GTM-IO8	b34	b33	GTM-IO0
GTM-IO9	b36	b35	GTM-IO1
GTM-IO10	b38	b37	GTM-IO2
GTM-IO11	b40	b39	GTM-IO3
not connected	b42	b41	GTM-IO4
not connected	b44	b43	GTM-IO5
not connected	b46	b45	GTM-IO6
not connected	b48	b47	GTM-IO7
CSWDG# (*1)	b50	b49	GND
not connected	b52	b51	GND

**Note!** (\*1) CSWDG# is not connected on Rev. 1 to 3 boards. This will be corrected in the next revision (Rev.4)!

## 12. USB & UART Interface ST2-Connector Pin out:

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

<i>VEE Core (*2)</i>	c2	c1	GND
<i>VFF RAM (*2)</i>	c4	c3	GND
MPH1-D0	c6	c5	MPH0-D0
MPH1-D1	c8	c7	MPH0-D1
MPH1-D2	c10	c9	MPH0-D2
MPH1-D3	c12	c11	MPH0-D3
MPH1-D4	c14	c13	MPH0-D4
MPH1-D5	c16	c15	MPH0-D5
MPH1-D6	c18	c17	MPH0-D6
MPH1-D7	c20	c19	MPH0-D7
MPH1-NXT	c22	c21	MPH0-NXT
MPH1-DIR	c24	c23	MPH0-DIR
MPH1-STP	c26	c25	MPH0-STP
MPH1-PWFLT	c28	c27	MPH0-PWFLT
MPH1-PCTL0	c30	c29	MPH0-PCTL0
MPH1-PCTL1	c32	c31	MPH0-PCTL1
MPH1-CLK	c34	c33	MPH0-CLK
GND	c36	c35	GND
GND	c38	c37	GND
CS0E	c40	c39	STDBY
VDD	c42	c41	VDD
VDD	c44	c43	VDD
VDD	c46	c45	VDD
VDD	c48	c47	VDD
VDD	c50	c49	VDD
VDD	c52	c51	VDD

not connected	d2	d1	GND
not connected	d4	d3	GND
not connected	d6	d5	not connected
not connected	d8	d7	not connected
not connected	d10	d9	not connected
not connected	d12	d11	not connected
not connected	d14	d13	not connected
not connected	d16	d15	not connected
not connected	d18	d17	SPI-MOSI
not connected	d20	d19	SPI-MISO
GND	d22	d21	SPI-SEL
GND	d24	d23	SPI-CLK
not connected	d26	d25	not connected
not connected	d28	d27	not connected
not connected	d30	d29	not connected
not connected	d32	d31	not connected
UTXD1	d34	d33	I2C1-SDA
URXD1	d36	d35	I2C1-SCL
<u>URTS1(*1)</u>	d38	d37	I2C2-SDA
<u>UCTS1(*1)</u>	d40	d39	I2C2-SCL
not connected	d42	d41	not connected
UTXD2	d44	d43	not connected
URXD2	d46	d45	not connected
<u>URTS2(*1)</u>	d48	d47	not connected
<u>UCTS2(*1)</u>	d50	d49	GND
not connected	d52	d51	GND

**Note!** (\*1) URTS1 vs. UCTS1 and URTS2 vs. UCTS2 are erroneously swapped on MPX8349 Rev.1+ 2, compared to the MPX standard. This is corrected in Rev.3.

(\*2) **Do not connect.** These Pins are connected to power planes via 1K resistors for test purposes only!

## DDR SDRAM Memory

The DDR SDRAM memory of the MPX8349 consists of four 16bit wide devices with a capacity of 256 MByte, offer an 8 bit wide ECC and is accessed via the MCS0# select line of the MPC8349E processor. The used DRAM types have an organization of 13 row and 10 column addresses and the four chip internal banks are accessed via the MBA0 and MBA1 signals.

### 12.1. Memory Bus Pin Configuration

<b>MPC8349E Signal</b>	<b>DDR-SDRAM Function</b>
MDQ(63:0)	Data Bus
MECC(7:0)	ECC Data Bus
MDM(8:0)	Data Mask
MDQS(8:0)	Data Strobe
MBA(1:0)	Bank Select
MBA2	not used
MA(12:0)	Address-Bus
MA(14:13)	not used
MCAS#	Column Address
MRAS#	Row Address
MWE#	Write Enable
MCS0#	Chip Select
MCS(3:1)#	not used
MVREF	Reference Voltage
MCKE0	Clock Enable
MCKE1	not used
MCLK(0:4) / MCLK(0:4)#	DRAM Clock
MCLK5 / MCLK5#	not used
ODT(3:0)	not used

## 12.2. Memory Bound CS0-BNDS

MSB	Name	Description	Value	Selection	HEX	
Bit 0	---	reserved	0		0	
Bit 1	---		0			
Bit 2	---		0			
Bit 3	---		0			
Bit 4	---	reserved	0		0	
Bit 5	---		0			
Bit 6	---		0			
Bit 7	---		0			
Bit 8	SA	Starting Address	0	Address bit MSB	0	
Bit 9	SA		0			
Bit 10	SA		0			
Bit 11	SA		0			
Bit 12	SA	Starting Address	0		0	
Bit 13	SA		0			
Bit 14	SA		0			
Bit 15	SA		0	Address bit LSB		
Bit 16	---	reserved	0		0	
Bit 17	---		0			
Bit 18	---		0			
Bit 19	---		0			
Bit 20	---	reserved	0		0	
Bit 21	---		0			
Bit 22	---		0			
Bit 23	---		0			
Bit 24	EA	Ending Address	0	Address bit MSB	0	
Bit 25	EA		0			
Bit 26	EA		0			
Bit 27	EA		0			
Bit 28	EA	Ending Address	1	256MByte	F	
Bit 29	EA		1			
Bit 30	EA		1			
Bit 31	EA		1	Address bit LSB		
LSB	name	description	value	selection	HEX	

### 12.3. Chips Select Configuration CS0-CONFIG

MSB	Name	Description	Value	Selection	HEX
Bit 0	CS0-EN	chip select enable	1	active	8
Bit 1	---	reserved	0		
Bit 2	---		0		
Bit 3	---		0		
Bit 4	---	reserved	0		0
Bit 5	---		0		
Bit 6	---		0		
Bit 7	---		0		
Bit 8	AP0-EN	auto precharge enable	1	not active	0
Bit 9	---	reserved	0		
Bit 10	---		0		
Bit 11	---		0		
Bit 12	---	reserved	0		0
Bit 13	---		0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	---	reserved	0		1
Bit 21	ROW-BITS	Number of Row Address Lines	0	13 Row Addresses	
Bit 22	ROW-BITS		0		
Bit 23	ROW-BITS		1		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	---	reserved	0		2
Bit 29	COL-BITS	Number of Column Address Lines	0	10 Column Addresses	
Bit 30	COL-BITS		1		
Bit 31	COL-BITS		0		
<b>LSB</b>	<b>name</b>	<b>description</b>	<b>value</b>	<b>selection</b>	<b>HEX</b>

## 12.4. DDR SDRAM Timing Configuration Timing-CFG-1

MSB	Name	Description	Value	Selection	HEX
Bit 0	---	reserved	0		
Bit 1	PRETOACT	Precharge to Activate	1	4 Clock Cycles	4
Bit 2	PRETOACT		0		
Bit 3	PRETOACT		0		
Bit 4	ACTTOPRE	Activate to Precharge	0	7 Clock Cycles	7
Bit 5	ACTTOPRE		1		
Bit 6	ACTTOPRE		1		
Bit 7	ACTTOPRE		1		
Bit 8	---	reserved	0		
Bit 9	ACTTORW	Activate to R/W	1	4 Clock Cycles	4
Bit 10	ACTTORW		0		
Bit 11	ACTTORW		0		
Bit 12	---	reserved	0		
Bit 13	CASLAT	CAS Latency	1	2,5 Clock Cycles	4
Bit 14	CASLAT		0		
Bit 15	CASLAT		0		
Bit 16	REFREC	Refresh recovery	0	12 Clock Cycles	4
Bit 17	REFREC		1		
Bit 18	REFREC		0		
Bit 19	REFREC		0		
Bit 20	---	reserved	0		
Bit 21	WRREC	Last data to precharge	0	3 Clock Cycles	3
Bit 22	WRREC		1		
Bit 23	WRREC		1		
Bit 24	---	reserved	0		
Bit 25	ACTTOACT	Activate-to-activate	0	2 Clock Cycles	2
Bit 26	ACTTOACT		1		
Bit 27	ACTTOACT		0		
Bit 28	---	reserved	0		
Bit 29	WRTORD	Last write data pair to read	0	1 Clock Cycle	1
Bit 30	WRTORD		0		
Bit 31	WRTORD		1		
LSB	name	description	value	selection	HEX

## 12.5. DDR SDRAM Timing Configuration Timing-CFG-2

MSB	name	description	value	selection	HEX
Bit 0	---	reserved	0		0
Bit 1	---		0		
Bit 2	---		0		
Bit 3	---		0		
Bit 4	CPO	MCAS-to-preamble override	0	CASLAT+1	0
Bit 5	CPO		0		
Bit 6	CPO		0		
Bit 7	CPO		0		
Bit 8	---	reserved	0		0
Bit 9	---		0		
Bit 10	---		0		
Bit 11	---		0		
Bit 12	ACSM	Address & control shift mode	0	normal Operation	0
Bit 13	---	reserved	0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	WRD-DLY		0		
Bit 20	WRD-DLY		1	4/8 Clock Delay	8
Bit 21	WRD-DLY		0		
Bit 22	---	reserved	0		
Bit 23	---		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	---	reserved	0		0
Bit 29	---		0		
Bit 30	---		0		
Bit 31	---		0		
LSB	name	description	value	selection	HEX

## 12.6. DDR SDRAM Control Configuration DDR-SDRAM-CFG

MSB	Name	Description	Value	Selection	HEX
Bit 0	MEM-EN	SDRAM interface enable	1	SDRAM active	C
Bit 1	SR-EN	Self refresh enable	1	not used	
Bit 2	ECC-EN	ECC enable	0	ECC not active	
Bit 3	RD-EN	Registered DIMM enable	0	not used	
Bit 4	---	reserved	0		2
Bit 5	---		0		
Bit 6	SDR-TYPE	SDRAM TYPE	1	DDR1-SDRAM	
Bit 7	SDR-TYPE		0		
Bit 8	---	reserved	0		0
Bit 9	---		0		
Bit 10	DYN-PWR	Dynamic power management	0	not used	
Bit 11	---	reserved	0		
Bit 12	---	reserved	0		0
Bit 13	---		0		
Bit 14	NCAP	Non-concurrent auto precharge	0	Concurrent Modus	
Bit 15	---	reserved	0		
Bit 16	2T-EN	2T timing enable	1	2T-Modus	8
Bit 17	---	reserved	0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	---	reserved	0		0
Bit 21	---		0		
Bit 22	---		0		
Bit 23	---		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	---	reserved	0		0
Bit 29	---		0		
Bit 30	---		0		
Bit 31	---		0		
LSB	Name	Description	Value	Selection	HEX

## 12.7. DDR SDRAM Interval Configuration DDR-SDRAM-INTERVAL

MSB	Name	Description	Value	Selection	HEX
Bit 0	---	reserved	0		0
Bit 1	---		0		
Bit 2	REFINT	refresh interval	0		
Bit 3	REFINT		0		
Bit 4	REFINT	refresh interval	0		5
Bit 5	REFINT		1		
Bit 6	REFINT		0		
Bit 7	REFINT		1		
Bit 8	REFINT	refresh interval	0	7.78us @ ...MHZ CCB Clock	1
Bit 9	REFINT		0		
Bit 10	REFINT		0		
Bit 11	REFINT		1		
Bit 12	REFINT	refresh interval	0		6
Bit 13	REFINT		1		
Bit 14	REFINT		1		
Bit 15	REFINT		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	BSTOPRE	precharge interval	0		
Bit 19	BSTOPRE		0		
Bit 20	BSTOPRE	precharge interval	0	t.b.d.	1
Bit 21	BSTOPRE		0		
Bit 22	BSTOPRE		0		
Bit 23	BSTOPRE		1		
Bit 24	BSTOPRE	precharge interval	0	t.b.d.	0
Bit 25	BSTOPRE		0		
Bit 26	BSTOPRE		0		
Bit 27	BSTOPRE		0		
Bit 28	BSTOPRE	precharge interval	0	t.b.d.	0
Bit 29	BSTOPRE		0		
Bit 30	BSTOPRE		0		
Bit 31	BSTOPRE		0		
LSB	name	description	value	selection	HEX

## 12.8. DDR SDRAM Mode Configuration Register DDR-SDRAM-MODE

MSB	name	description	value	selection	HEX	
Bit 0		Extended SDRAM-Mode	0	set to EMRS	4	
Bit 1	MRS/EMRS		1			
Bit 2			0			
Bit 3			0			
Bit 4	operating mode	Extended SDRAM-Mode	0		0	
Bit 5	operating mode		0			
Bit 6	operating mode		0			
Bit 7	operating mode		0			
Bit 8	operating mode	Extended SDRAM-Mode	0		0	
Bit 9	operating mode		0			
Bit 10	operating mode		0			
Bit 11	operating mode		0			
Bit 12	operating mode	Extended SDRAM-Mode	0		2	
Bit 13	operating mode		0			
Bit 14	drive strength		1			half strength driver
Bit 15	DLL enable		0			DLL enabled
Bit 16		SDRAM-Mode	0	set to MRS	0	
Bit 17	MRS/EMRS		0			
Bit 18			0			
Bit 19			0			
Bit 20	operating mode	SDRAM-Mode	0	normal operation	0	
Bit 21	operating mode		0			
Bit 22	operating mode		0			
Bit 23	operating mode		0			
Bit 24	operating mode	SDRAM-Mode	0	CAS Latency = 2.5	6	
Bit 25	CAS latency		1			
Bit 26	CAS latency		1			
Bit 27	CAS latency		0			
Bit 28	burst type	SDRAM-Mode	0	Sequential	2	
Bit 29	burst length		0	Burst Length 4		
Bit 30	burst length		1			
Bit 31	burst length		0			
LSB	name	description	value	selection	HEX	

## 13. Flash Memory

The flash memory of the MPX8349 consists of a single device with a 16-bit wide data bus. The used device S29GL128M90F from SPANSION is controlled via select line LCS0#, the LGPL2 line and the LWE0# line by the GPCM of the MPC8349E. It can be disabled by setting the LCSE# line on connector ST2-c40 to high. The flash device is reset by power-up or key-reset. It is not affected by a CPU initiated reset. The CPU cannot detect the RDY/BSY line of the device.

### 13.1. Base Register BR0

MSB	Name	Description	Value	Selection	HEX
Bit 0	BA	Base Address	1	base address bit MSB	F
Bit 1	BA		1		
Bit 2	BA		1		
Bit 3	BA		1		
Bit 4	BA	Base Address	1		C
Bit 5	BA		1		
Bit 6	BA		0		
Bit 7	BA		0		
Bit 8	BA	Base Address	0		0
Bit 9	BA		0		
Bit 10	BA		0		
Bit 11	BA		0		
Bit 12	BA	Base Address	0		0
Bit 13	BA		0		
Bit 14	BA		0		
Bit 15	BA		0		
Bit 16	BA	Base Address	0	base address bit LSB	1
Bit 17	---	reserved, must be 0	0		
Bit 18	---	reserved, must be 0	0		
Bit 19	PS	Port Size	1	16 Bit	0
Bit 20	PS	Port Size	0	16 Bit	
Bit 21	---	reserved, must be 0	0		
Bit 22	---		0		
Bit 23	WP	Write Protect	0	not write protected	
Bit 24	MS	Machine Select	0	GPCM 60x-Bus	0
Bit 25	MS		0		
Bit 26	MS		0		
Bit 27	MEMEC	external MEMEC enable	0	internal controller	
Bit 28	ATOM	Atomic Operation	0	not used	1
Bit 29	ATOM		0		
Bit 30	DR	Data Pipelining	0	no pipelining	
Bit 31	V	Valid Bit	1	1 = CS active	
LSB	name	description	value	selection	HEX

### 13.2. Option Register OR0

MSB	name	description	value	selection	HEX
Bit 0	AM	Address Mask	1	address mask MSB	F
Bit 1	AM		1		
Bit 2	AM		1		
Bit 3	AM		1		
Bit 4	AM	Address Mask	1		F
Bit 5	AM		1		
Bit 6	AM		1		
Bit 7	AM		1		
Bit 8	AM	Address Mask	0		0
Bit 9	AM		0		
Bit 10	AM		0		
Bit 11	AM		0		
Bit 12	AM	Address Mask	0		0
Bit 13	AM		0		
Bit 14	AM		0		
Bit 15	AM		0		
Bit 16	AM	Address Mask	0	address mask LSB	0
Bit 17	--	reserved, must be 0	0		
Bit 18	--	reserved, must be 0	0		
Bit 19	BCTLD	Data Buffer Control Disable	0	LBCTL & LWR active	
Bit 20	CSNT	Chip Select Negation Time	1	¼ clock earlier	C
Bit 21	ACS	Address to CS Setup	1	same timing	
Bit 22	ACS		0		
Bit 23	XACS	extended ACS	0	extended setup	
Bit 24	SCY	Cycle Length in Clocks	0	2 waitstates	2
Bit 25	SCY		0		
Bit 26	SCY		1		
Bit 27	SCY		0		
Bit 28	SETA	External Termination	0	internal termination	2
Bit 29	TRLX	Timing Relaxed	0	8 clocks idle	
Bit 30	EHTR	extended Hold time on Read	1		
Bit 31	EAD	external address latch delay	0	extra cycles added	
LSB	name	description	value	selection	HEX

## 14. SRAM

The static RAM of the MPX8349 consists of a single device with a 16-bit wide data bus. The used device CS16LV40963 from CHIPLUS is controlled via select line LCS1#, the LGPL1 and the LGPL2 line via one of the UPMs of the MPC8349E. The data contents of the SRAM device is protected by a local gold capacitor, which is also used to keep the onboard RTC running during short power down periods.

### 14.1. SRAM Pin Configuration

<b>MPC8349E Signal</b>	<b>Function</b>	<b>SRAM Signal</b>
LAD15-LAD0	Data-Bus	D0-D15
LCS1#	Chip Select	CE
LGPL1	Write Enable	WE
LGPL2	Read Enable	OE
LWE(1-0)	Byte Enable	LB/UB
LA30-LA12	Address-Bus	A0-A18

## 14.2. Base Register BR1

MSB	name	description	value	selection	HEX
Bit 0	BA	Base Address	1	Base Address bit MSB	F
Bit 1	BA		1		
Bit 2	BA		1		
Bit 3	BA		1		
Bit 4	BA	Base Address	0		0
Bit 5	BA		0		
Bit 6	BA		0		
Bit 7	BA		0		
Bit 8	BA	Base Address	0		0
Bit 9	BA		0		
Bit 10	BA		0		
Bit 11	BA		0		
Bit 12	BA	Base Address	0		0
Bit 13	BA		0		
Bit 14	BA		0		
Bit 15	BA		0		
Bit 16	BA	Base Address	0	Base Address bit LSB	1
Bit 17	---	reserved, must be 0	0	not used	
Bit 18	---	reserved, must be 0	0	not used	
Bit 19	PS	Port Size	1	16 Bit	
Bit 20	PS	Port Size	0	16 Bit	0
Bit 21	DECC	Data Error Correction	0	no Parity/ECC	
Bit 22	DECC		0		
Bit 23	WP	Write Protect	0	not write protected	
Bit 24	MS	Machine Select	1	UPMA	8
Bit 25	MS		0		
Bit 26	MS		0		
Bit 27	---	reserved	0	not used	
Bit 28	ATOM	Atomic Operation	0	not used	1
Bit 29	ATOM		0		
Bit 30	---	reserved	0	not used	
Bit 31	V	Valid Bit	1	1 = CS active	
LSB	name	description	value	selection	HEX

### 14.3. Option Register OR1

MSB	name	description	value	selection	HEX
Bit 0	AM	Address Mask	1	Address Mask MSB	F
Bit 1	AM		1		
Bit 2	AM		1		
Bit 3	AM		1		
Bit 4	AM	Address Mask	1		F
Bit 5	AM		1		
Bit 6	AM		1		
Bit 7	AM		1		
Bit 8	AM	Address Mask	1		F
Bit 9	AM		1		
Bit 10	AM		1		
Bit 11	AM		1		
Bit 12	AM	Address Mask	1		8
Bit 13	AM		0		
Bit 14	AM		0		
Bit 15	AM		0		
Bit 16	AM	Address Mask	0	Address Mask LSB	0
Bit 17	--	reserved, must be 0	0	not used	
Bit 18	--	reserved, must be 0	0	not used	
Bit 19	BCTLD	Data Buffer Control Disable	0	LBCTL active	
Bit 20	--	reserved, must be 0	0	not used	1
Bit 21	--	reserved, must be 0	0	not used	
Bit 22	--	reserved, must be 0	0	not used	
Bit 23	BI	Burst Inhibit	1	no Burst Access	
Bit 24	--	reserved, must be 0	0	not used	0
Bit 25	--	reserved, must be 0	0	not used	
Bit 26	--	reserved, must be 0	0	not used	
Bit 27	--	reserved, must be 0	0	not used	
Bit 28	--	reserved, must be 0	0	not used	0
Bit 29	TRLX	Timing Relax	0	normal Timing	
Bit 30	EHTR	extended Hold time on Read	0		
Bit 31	EAD	external address latch delay	0	LALE = 1 Clock	
LSB	Name	Description	Value	Selection	HEX

## 15. DiskOnChip

There is a DiskOnChip device onboard of the MPX8349. It consists of a single device with a 16-bit wide data bus. The optional used device MD2533-d1G (128MB) (MD2433-DBG-V3Q18 used on Rev. 1 and Rev. 2) from M-SYSTEMS / Sandisk is controlled via select line LCS2#, the LGPL1 and the LGPL2 line via one of the UPMs of the MPC8349E. Optional the IRQ line of the device can be connected to IRQ3# via soldering link DOC.

### 15.1. DiskOnChip Pin Configuration

MPC8349E Signal	Function	DiskOnChip Signal
LAD15 - LAD8	Data-Bus	D8 - D15
LAD7 - LAD0	Data-Bus	D7 - D0
LCS2#	Chip Select	CE
LGPL1	Write Enable	WE
LGPL2	Read Enable	OE
LCLK1	Clock	CLK
---	---	A0 tied to low
LA30-LA19	Address-Bus	A1-A12
IRQ3#	Interrupt	IRQ connected to IRQ3# via DOC
HRST	Reset	RST
---	not used	DRQ tied to high
---	not used	DBSY tied to high
---	not used	LCK tied to high
---	16 bit mode	CFG tied to high

## 15.2. Base Register BR2

MSB	Name	Description	Value	Selection	HEX
Bit 0	BA	Base Address	1	Base Address bit MSB	F
Bit 1	BA		1		
Bit 2	BA		1		
Bit 3	BA		1		
Bit 4	BA	Base Address	0		1
Bit 5	BA		0		
Bit 6	BA		0		
Bit 7	BA		1		
Bit 8	BA	Base Address	0		0
Bit 9	BA		0		
Bit 10	BA		0		
Bit 11	BA		0		
Bit 12	BA	Base Address	0		0
Bit 13	BA		0		
Bit 14	BA		0		
Bit 15	BA		0		
Bit 16	BA	Base Address	0	Base Address bit LSB	1
Bit 17	---	reserved, must be 0	0	not used	
Bit 18	---	reserved, must be 0	0	not used	
Bit 19	PS	Port Size	1	16 Bit	
Bit 20	PS	Port Size	0	16 Bit	0
Bit 21	DECC	Data Error Correction	0	no Parity/ECC	
Bit 22	DECC		0		
Bit 23	WP	Write Protect	0	not write protected	
Bit 24	MS	Machine Select	1	UPMB	8
Bit 25	MS		0		
Bit 26	MS		1		
Bit 27	---	reserved	0	not used	
Bit 28	ATOM	Atomic Operation	0	not used	1
Bit 29	ATOM		0		
Bit 30	---	reserved	0	not used	
Bit 31	V	Valid Bit	1	1 = CS active	
LSB	Name	Description	Value	Selection	HEX

### 15.3. Option Register OR2

MSB	Name	Description	Value	Selection	HEX
Bit 0	AM	Address Mask	1	Address Mask MSB	F
Bit 1	AM		1		
Bit 2	AM		1		
Bit 3	AM		1		
Bit 4	AM	Address Mask	1		F
Bit 5	AM		1		
Bit 6	AM		1		
Bit 7	AM		1		
Bit 8	AM	Address Mask	1		F
Bit 9	AM		1		
Bit 10	AM		1		
Bit 11	AM		1		
Bit 12	AM	Address Mask	0		0
Bit 13	AM		0		
Bit 14	AM		0		
Bit 15	AM		0		
Bit 16	AM	Address Mask	0	Address Mask LSB	0
Bit 17	--	reserved, must be 0	0	not used	
Bit 18	--	reserved, must be 0	0	not used	
Bit 19	BCTLD	Data Buffer Control Disable	0	LBCTL active	
Bit 20	--	reserved, must be 0	0	not used	1
Bit 21	--	reserved, must be 0	0	not used	
Bit 22	--	reserved, must be 0	0	not used	
Bit 23	BI	Burst Inhibit	1	no Burst Access	
Bit 24	--	reserved, must be 0	0	not used	0
Bit 25	--	reserved, must be 0	0	not used	
Bit 26	--	reserved, must be 0	0	not used	
Bit 27	--	reserved, must be 0	0	not used	
Bit 28	--	reserved, must be 0	0	not used	0
Bit 29	TRLX	Timing Relax	0	normal Timing	
Bit 30	EHTR	extended hold time on Read	0		
Bit 31	EAD	external address latch delay	0	LALE = 1 Clock	
LSB	Name	Description	Value	Selection	HEX

## 16. I<sup>2</sup>C EEPROM

### 16.1. EEPROM I<sup>2</sup>C Access Address

<b>Device</b>	<b>Hex</b>	<b>Binary I<sup>2</sup>C address</b>						<b>Read/write</b>	
AT24C128	A6/A7	1	0	1	0	0	1	1	1/0

The AT24C128 uses a two 8-bit address words following the shown device address for data access. The write protect function of the Atmel EEPROM device is disabled.

## 17. Real Time Clock PCF8563T

### 17.1. RTC I<sup>2</sup>C Access Address

<b>Device</b>	<b>Hex</b>	<b>Binary I<sup>2</sup>C address</b>						<b>Read/write</b>	
PCF8563T	A2/A3	1	0	1	0	0	0	1	1/0

The PCF8563T uses an 8-bit address word following the shown device address for register and data access. The interrupt line of the RTC is not connected.

## 17.2. RTC Address Map

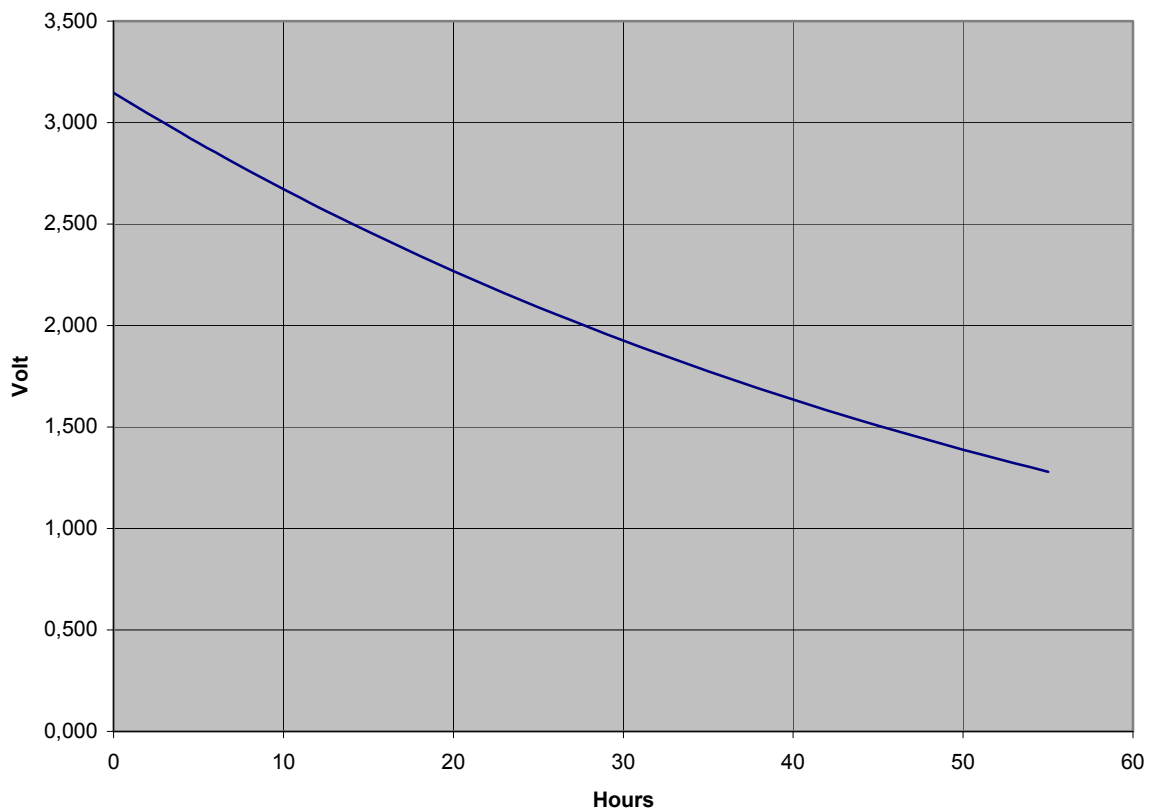
<b>Bit oriented registers</b>									
Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
\$00	Control/Status 1	TEST 1	0	STOP	0	TEST C	0	0	0
\$01	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
\$0D	CLKOUT frequency	FE	--	--	--	--	--	FD1	FD0
\$0E	Timer control	TE	--	--	--	--	--	TD1	TD0
\$0F	Timer countdown value	<timer countdown value>							

<b>BCD formatted registers</b>									
Address	Register name	D7	D6	D5	D4	D3	D2	D1	D0
		BCD format tens nibble				BCD format units nibble			
\$02	Seconds	VL	<Seconds 00 to 59 coded in BCD>						
\$03	Minutes	--	<Minutes 00 to 59 coded in BCD>						
\$04	Hours	--	--	<Hours 00 to 23 coded in BCD>					
\$05	Days	--	--	<Days 01 to 31 coded in BCD>					
\$06	Weekdays	--	--	--	--	--	<Weekday 0 to 6>		
\$07	Month/Century	C	--	--	<Month 01 to 12 coded in BCD>				
\$08	Years	<Years 00 to 99 coded in BCD>							
\$09	Minute alarm	AE	<Minute alarm 00 to 59 coded in BCD>						
\$0A	Hour alarm	AE	--	<Hour alarm 00 to 23 coded in BCD>					
\$0B	Day alarm	AE	--	<Day alarm 01 to 31 coded in BCD>					
\$0C	Weekday alarm	AE	--	--	--	--	<Weekday alarm 0 to 6>		

## 18. Data Retention

The primary data retention is performed by a local gold capacitor. Additional backup power can be supplied via signal STDBY on connector ST2-c39. The external supply voltage must not exceed 3.3V. The RTC PCF8563T works with a minimum supply voltage of 1.0 volt, while the SRAM devices needs at least 1.5 volts for data retention. The CLKOUT and timer of the PCF8563T should be disabled to reduce power consumption.

### 18.1. Capacitor Backup Time

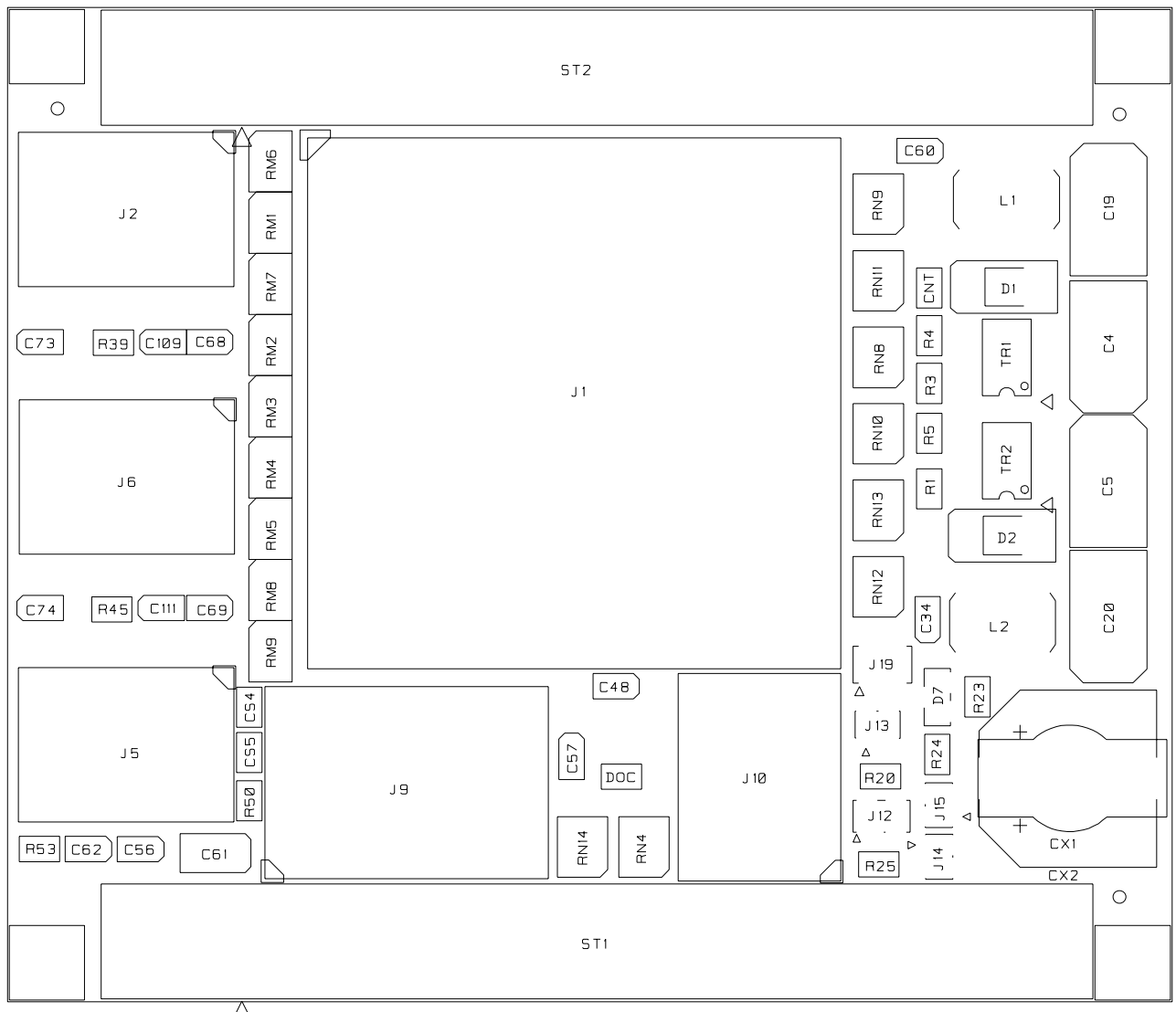


## 19. Hardware Watchdog Timer

The MPX8349 features a fixed rate hardware timer for watchdog purposes (MAX823), which can be enabled by software. Once enabled by a low active pulse (min. 50ns) to signal CSWDG#, it only can be disabled by a hardware reset. The time out rate is 1.6 seconds. Within that time at least one access must be performed to signal CSWDG#, to retrigger the timer. The signal CSWDG# leads to connector ST2, Pin B50 and must be connected to a software controllable signal on the carrier board. Leaving this pin open disables the watchdog timer.

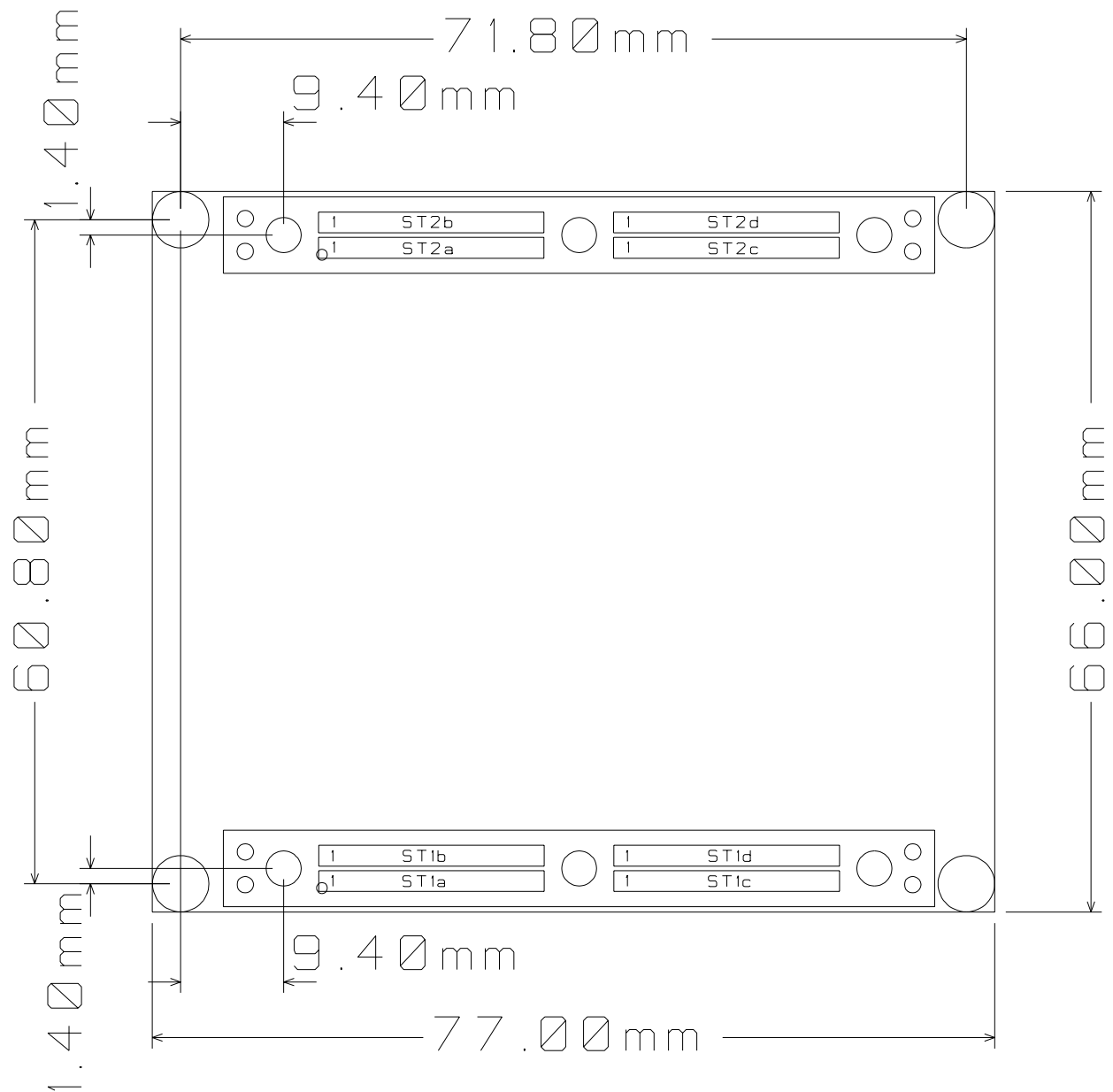
## Appendices

## Layout Component Side





## Physical Dimensions (Top View)



## **Schematics MPX8349 (please contact *MicroSys*)**