

# **Microsys**

**User's Manual**

**MPX5200 Rev. 1**

**preliminary**

# Declaration of Conformity

We, Manufacturer  
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Germany

declare that the product

**MPX5200**

is in conformity with:

**EN 50081-1 Generic emission standard**  
**EN 50082-1 Generic immunity standard**

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position:       General Manager

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## Chip Select Overview

signal	function	bus width	mode	size	description
CS0	FLASH	8 Bit	GPCM	16 MByte	
CS1	SRAM	8 Bit	GPCM	2 MByte	
CS2	DiskOnChip	8 Bit	GPCM	1 MByte	
CS3	ST1 b24	---	---	---	not used onboard
CS4	ST1 b26	---	---	---	not used onboard
CS5	ST1 b28	---	---	---	not used onboard

## Addressmap

Type	Base	End	Select	Bus	Size
<b>MPC5200 Internal Ram (MBAR)</b>	<b>\$F000 0000</b>	<b>\$F000 7FFF</b>			
SDRAM	\$0000 0000	\$03FF FFFF	MCS0	603	32Bit
Flash	\$FC00 0000	\$FCFF FFFF	CS0	LocalPlus	8Bit
SRAM	\$F100 0000	\$F11F FFFF	CS1	LocalPlus	8Bit
DiskOnChip	\$E000 0000	\$E00F FFFF	CS2	LocalPlus	8Bit
not initialized			CS3		
not initialized			CS4		
not initialized			CS5		

## I2C Address Overview:

Device:	Hex:	binary I <sup>2</sup> C address							read/write
PCF8563T	A2/A3	1	0	1	0	0	0	1	1/0
AT24C128	A6/A7	1	0	1	0	0	1	1	1/0

## Power Supply Ratings:

The MPX5200 module must be supplied with single 3.3V and all pins of the module are 3.3V tolerant only. There is a 12 pin wide VDD supply block on connector ST2-C and several GND pins distributed over connector ST1 and ST2. For a proper operation, all ground pins and all VDD pins should be connected to the carrier board.

<b>3.3V</b>	<b>ST2-C</b>	<b>ST2-C</b>	<b>3.3V</b>
VDD	pin c41	pin c42	VDD
VDD	pin c43	pin c44	VDD
VDD	pin c45	pin c46	VDD
VDD	pin c47	pin c48	VDD
VDD	pin c49	pin c50	VDD
VDD	pin c51	pin c52	VDD

<b>name</b>	<b>rating</b>	<b>current</b>	<b>tolerance</b>	<b>ripple</b>
VDD	+3.3VDC	peak 1A	+/-5%	max.50mV

## The Backup Supply Ratings:

The MPX5200 contains a realtime clock and two static ram devices. The data contents of all devices can be saved during short power down periods by the onboard gold capacitor. For extended backup times an external power can be supplied via the STDBY line.

<b>3.3V</b>	<b>ST2-C</b>
STDBY	c39

<b>name</b>	<b>rating</b>	<b>current</b>	<b>tolerance</b>	<b>ripple</b>
STDBY	+3.3VDC	max. 5uA	+/-10%	max.50mV

## The MPC5200B Processor

The MPC5200B cpu is connected to a 32 bit wide DDR SDRAM. The local bus side handles the onboard Flash, SRAM, and the DiskOnChip device by the select lines CS0, CS1 and CS2, i.e. CS3, CS4 and CS5 can be used for other purposes.

### ***BDM JTAG Port Connection:***

The JTAG port of the MPC5200B can be accessed via ST2-A by the following signals :

signal	ST2-A	ST2-A	signal	description
TMS	pin c33	pin c34		
TDI	pin c35	pin c36	CKSTO	MPC5200B signal TEST_SEL0
TDO	pin c37			
TCK	pin c39	pin c40	HRST#	
TRST#	pin c41	pin c42	SRST#	

During normal operation, the TRST# signal is controlled by an onboard logic, i.e. no external connections are necessary.

## Interrupt Configuration:

MPC5200B Signal	Destination	onboard source
IRQ0#	ST2-a43	---
IRQ1#	ST2-a45	---
IRQ2#	ST2-a47	Real-Time-Clock IRQ via link R12
IRQ3#	ST2-a44	DiskOnChip IRQ via link R8

## Reset Configuration Signals:

For proper operation, the MPC5200B needs several signal for a functional configuration during power up. These signals are tied to high or low via 4K7 pullup or pulldown resistors. In case an external circuitry drives these signals during power up or there are additional pullup or pulldown resistors on the carrier board, the necessary configuration can not been performed.

Signal	Destination	Reset Function	Link	Normal Function
ATA-DACK#	ST1-a42	ppc-pll-config-4	CFL0/CFH0	ATA dma acknowledge
ATA-IOR#	ST1-b33	ppc-pll-config-3	CFL1/CFH1	ATA IO read
ATA-IOW#	ST1-b35	ppc-pll-config-2	CFL2/CFH2	ATA IO write
LWE#	ST1-b19	ppc-pll-config-1	CFL3/CFH3	local bus write
LALE	ST1-b15	ppc-pll-config-0	CFL4/CFH4	local bus address latch
LTS#	ST1-b23	xlclk-sel	CFL5/CFH5	local bus cycle start
USB1-1	ST2-d4	sys-pll-config-0	CFL6/CFH6	USB-TXN
USB1-2	ST2-d6	sys-pll-config-1	CFL7/CFH7	USB-TXP
ETH-0	ST2-a4	boot-rom-mg	CFL8/CFH8	ETH-TXEN
ETH-1	ST2-a5	large-flash-select	CFL9/CFH9	ETH-TXD0
ETH-2	ST2-a6	ppc-msrip	CFL10/CFH10	ETH-TXD1
ETH-3	ST2-a7	boot-rom-wait	CFL11/CFH11	ETH-TXD2
ETH-4	ST2-a8	boot-rom-swap	CFL12/CFH12	ETH-TXD3
ETH-5	ST2-a21	boot-rom-size	CFL13/CFH13	ETH-TXER
ETH-6	ST2-a29	boot-rom-type	CFL14/CFH14	ETH-MDC

## Local-Bus:

The local bus of the MPX5200 is accessible via the connectors ST1-A and ST1-B. All local bus lines are connected, even if some of them are used by onboard devices.

### Local-Bus Pin Configuration:

MPC5200B Signal	Destination	onboard function
LAD(31:0)	ST1-A	Address/Data Bus
LCS0	ST1-b18	Flash Chip Select
LCS1	ST1-b20	SRAM Chip Select
LCS2	ST1-b22	DiskOnChip Select
LCS3	ST1-b24	not used
LCS4	ST1-b26	not used
LCS5	ST1-b28	not used
LALE	ST1-b15	not used
GPIO-WAKEUP7	ST1-b17	not used
LWE#	ST1-b19	Flash / SRAM / DiskOnChip
LOE#	ST1-b21	Flash / SRAM / DiskOnChip
LTS#	ST1-b23	not used
LACK#	ST1-b25	not used
TEST_SEL1	ST1-b27	not used
PCICLK	ST1-b52	DiskOnChip

## Local Bus ST1-Connector Pin out:

Location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

AD8	a2	a1	GND
AD9	a4	a3	GND
AD10	a6	a5	AD0
AD11	a8	a7	AD1
AD12	a10	a9	AD2
AD13	a12	a11	AD3
AD14	a14	a13	AD4
AD15	a16	a15	AD5
GND	a18	a17	AD6
GND	a20	a19	AD7
AD24	a22	a21	AD16
AD25	a24	a23	AD17
AD26	a26	a25	AD18
AD27	a28	a27	AD19
AD28	a30	a29	AD20
AD29	a32	a31	AD21
AD30	a34	a33	AD22
AD31	a36	a35	AD23
ATA-ISOLATE	a38	a37	GND
ATA-DRQ	a40	a39	GND
ATA-DACK#	a42	a41	ATA-INTRQ
not connected	a44	a43	not connected
not connected	a46	a45	not connected
not connected	a48	a47	not connected
GND	a50	a49	not connected
GND	a52	a51	not connected

not connected	b2	b1	GND
not connected	b4	b3	GND
not connected	b6	b5	not connected
not connected	b8	b7	not connected
not connected	b10	b9	not connected
not connected	b12	b11	not connected
not connected	b14	b13	not connected
not connected	b16	b15	LALE
CS0#	b18	b17	GPIO-WAKEUP7
CS1#	b20	b19	LWE#
CS2#	b22	b21	LOE#
CS3#	b24	b23	LTS#
CS4#	b26	b25	LACK#
CS5#	b28	b27	TEST-SEL1
not connected	b30	b29	not connected
GND	b32	b31	not connected
GND	b34	b33	ATA-IOR#
ATA-IOCHRDY	b36	b35	ATA-IOW#
not connected	b38	b37	not connected
A-GNT0#	b40	b39	A-REQ0#
not connected	b42	b41	not connected
not connected	b44	b43	not connected
not connected	b46	b45	not connected
not connected	b48	b47	not connected
A-RST	b50	b49	GND
A-PCICLK0	b52	b51	GND

## PCI-Interface:

The MPX5200 offers a simple 32bit PCI interface located on connector ST1-D. The according clock and the two arbiter signals are located on the connector ST1-B. All PCI relevant signals of the MPC5200B are available as external connections.

### PCI-Bus Clock Configuration:

MPC5200B Signal	Destination	Function
PCICLK-0	ST2-b52	Reference clock for local bus & PCI

### PCI Bus ST1-Connector Pin out:

Location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

**PCI Bus ST1-Connector Pin out:**

not connected	a38	a37	GND
not connected	a40	a39	GND
not connected	a42	a41	not connected
not connected	a44	a43	not connected
not connected	a46	a45	not connected
not connected	a48	a47	not connected
GND	a50	a49	not connected
GND	a52	a51	not connected

not connected	b38	b37	not connected
A-GNT0	b40	b39	A-REQ0
not connected	b42	b41	not connected
not connected	b44	b43	not connected
not connected	b46	b45	not connected
not connected	b48	b47	not connected
not connected	b50	b49	GND
A-PCICLK	b52	b51	GND

not connected	c2	c1	GND
not connected	c4	c3	GND
not connected	c6	c5	not connected
not connected	c8	c7	not connected
not connected	c10	c9	not connected
not connected	c12	c11	not connected
not connected	c14	c13	not connected
not connected	c16	c15	not connected
GND	c18	c17	not connected
GND	c20	c19	not connected
not connected	c22	c21	not connected
not connected	c24	c23	not connected
not connected	c26	c25	not connected
not connected	c28	c27	not connected
not connected	c30	c29	not connected
not connected	c32	c31	not connected
not connected	c34	c33	GND
not connected	c36	c35	GND
not connected	c38	c37	not connected
not connected	c40	c39	not connected
not connected	c42	c41	not connected
not connected	c44	c43	not connected
not connected	c46	c45	not connected
not connected	c48	c47	not connected
GND	c50	c49	not connected
GND	c52	c51	not connected

A-AD8	d2	d1	GND
A-AD9	d4	d3	GND
A-AD10	d6	d5	A-AD0
A-AD11	d8	d7	A-AD1
A-AD12	d10	d9	A-AD2
A-AD13	d12	d11	A-AD3
A-AD14	d14	d13	A-AD4
A-AD15	d16	d15	A-AD5
GND	d18	d17	A-AD6
GND	d20	d19	A-AD7
A-CBE1	d22	d21	A-CBE0
A-DVSL	d24	d23	A-FRME
A-PERR	d26	d25	A-IRDY
A-SERR	d28	d27	A-TRDY
A-PAR	d30	d29	A-STOP
A-CBE3	d32	d31	A-CBE2
A-AD24	d34	d33	GND
A-AD25	d36	d35	GND
A-AD26	d38	d37	A-AD16
A-AD27	d40	d39	A-AD17
A-AD28	d42	d41	A-AD18
A-AD29	d44	d43	A-AD19
A-AD30	d46	d45	A-AD20
A-AD31	d48	d47	A-AD21
GND	d50	d49	A-AD22
GND	d52	d51	A-AD23

all shaded PCI signals are tied to high by 10kOhm pullup resistors.

## MII Interface ST2-Connector Pin out:

Location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

not connected	a2	a1	GND
ETH-0	a4	a3	GND
ETH-2	a6	a5	ETH-1
ETH-4	a8	a7	ETH-3
ETH-12	a10	a9	not connected
ETH-14	a12	a11	ETH-13
ETH-9	a14	a13	ETH-15
ETH-17	a16	a15	ETH-8
not connected	a18	a17	not connected
not connected	a20	a19	not connected
not connected	a22	a21	ETH-5
not connected	a24	a23	not connected
ETH-16	a26	a25	not connected
ETH-11	a28	a27	ETH-10
GND	a30	a29	ETH-6
GND	a32	a31	ETH-7
not connected	a34	a33	JTMS
TEST-SEL0	a36	a35	JTDI
KRST#	a38	a37	JTDO
HRST#	a40	a39	JTCK
SRST#	a42	a41	JTRST#
IRQ3#	a44	a43	IRQ0#
not connected	a46	a45	IRQ1#
not connected	a48	a47	IRQ2#
not connected	a50	a49	GND
not connected	a52	a51	GND

EXT-CCLK	b2	b1	GND
not connected	b4	b3	GND
not connected	b6	b5	not connected
not connected	b8	b7	not connected
not connected	b10	b9	not connected
not connected	b12	b11	not connected
not connected	b14	b13	not connected
not connected	b16	b15	not connected
not connected	b18	b17	not connected
not connected	b20	b19	not connected
not connected	b22	b21	not connected
not connected	b24	b23	not connected
not connected	b26	b25	not connected
not connected	b28	b27	not connected
GND	b30	b29	not connected
GND	b32	b31	PRST#
not connected	b34	b33	TIMER-0
not connected	b36	b35	TIMER-1
not connected	b38	b37	TIMER-2
not connected	b40	b39	TIMER-3
not connected	b42	b41	TIMER-4
not connected	b44	b43	TIMER-5
GPIO-WAKEUP6	b46	b45	TIMER-6
GPIO-WAKEUP7	b48	b47	TIMER-7
CS-WDOG#	b50	b49	GND
not connected	b51	b52	GND

## USB & PSC Interface ST2-Connector Pin out:

Location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

VEE Core	c2	c1	GND
VFF RAM	c4	c3	GND
not connected	c6	c5	not connected
not connected	c8	c7	not connected
not connected	c10	c9	not connected
not connected	c12	c11	not connected
not connected	c14	c13	not connected
not connected	c16	c15	not connected
not connected	c18	c17	not connected
not connected	c20	c19	not connected
not connected	c22	c21	not connected
not connected	c24	c23	not connected
not connected	c26	c25	not connected
not connected	c28	c27	not connected
not connected	c30	c29	not connected
not connected	c32	c31	not connected
not connected	c34	c33	not connected
GND	c36	c35	GND
GND	c38	c37	GND
CS0E	c40	c39	STDBY
VDD	c42	c41	VDD
VDD	c44	c43	VDD
VDD	c46	c45	VDD
VDD	c48	c47	VDD
VDD	c50	c49	VDD
VDD	c52	c51	VDD

USB1-0	d2	d1	GND
USB1-1	d4	d3	GND
USB1-2	d6	d5	PSC3-0
USB1-3	d8	d7	PSC3-1
USB1-4	d10	d9	PSC3-2
USB1-5	d12	d11	PSC3-3
USB1-6	d14	d13	PSC3-4
USB1-7	d16	d15	PSC3-5
USB1-8	d18	d17	PSC3-6
USB1-9	d20	d19	PSC3-7
GND	d22	d21	PSC3-8
GND	d24	d23	PSC3-9
not connected	d26	d25	not connected
not connected	d28	d27	not connected
not connected	d30	d29	not connected
not connected	d32	d31	not connected
PSC1-0	d34	d33	I2C-1
PSC1-1	d36	d35	I2C-0
PSC1-2	d38	d37	I2C-3
PSC1-3	d40	d39	I2C-2
PSC1-4	d42	d41	PSC6-0
PSC2-0	d44	d43	PSC6-1
PSC2-1	d46	d45	PSC6-2
PSC2-2	d48	d47	PSC6-3
PSC2-3	d50	d49	GND
PSC2-4	d52	d51	GND

## DDR SDRAM Memory:

The DDR SDRAM memory of the MPX5200 consists of two 16bit wide devices with a total capacity of 64MByte, and is accessed via the MCS0# select line of the MPC5200B processor. The used DRAM types have an organization of 13 row and 10 column addresses and the four chip internal banks are accessed via the MBA0 and MBA1 signals.

### **Memory-Bus Pin Configuration:**

MPC5200B Signal	DDR-SDRAM Function
MDQ(32:0)	Data Bus
DQM(3:0)	Data Mask
MDQS(3:0)	Data Strobe
MBA(1:0)	Bank Select
MA(12:0)	Address-Bus
MCAS#	Column Address
MRAS#	Row Address
MWE#	Write Enable
MCS0#	Chip Select
MCS1#/GPIO-WAKEUP6	not used
MCKE	Clock Enable
MCLK / MCLK#	DRAM Clock

## Flash Memory

The flash memory of the MPX5200 consists of a single device and works in the 8 bit non-multiplexed mode with 24 address lines. The used device S29GL128M10FF from SPANSION is controlled via the select line CS0#, the LOE# line and the LWE# line by the local bus of the MPC5200B. It can be disabled by setting the LCSE# line on connector ST2-c40 to high. The flash device is reset by power-up or key-reset. It is not affected by a cpu initiated reset. The RDY/BSY line of the device can not be detected by the cpu.

### Chip-0-Select-Start-Address-Register

MSB	name	description	value	selection	HEX
Bit 0	Rsrvd	reserved	0		0
Bit 1	Rsrvd		0		
Bit 2	Rsrvd		0		
Bit 3	Rsrvd		0		
Bit 4	Rsrvd	reserved	0		0
Bit 5	Rsrvd		0		
Bit 6	Rsrvd		0		
Bit 7	Rsrvd		0		
Bit 8	Rsrvd	reserved	0		0
Bit 9	Rsrvd		0		
Bit 10	Rsrvd		0		
Bit 11	Rsrvd		0		
Bit 12	Rsrvd	reserved	0		0
Bit 13	Rsrvd		0		
Bit 14	Rsrvd		0		
Bit 15	Rsrvd		0		
Bit 16	SA	start address	1	start address bit MSB	F
Bit 17	SA		1		
Bit 18	SA		1		
Bit 19	SA		1		
Bit 20	SA	start address	1		C
Bit 21	SA		1		
Bit 22	SA		0		
Bit 23	SA		0		
Bit 24	SA	start address	0		0
Bit 25	SA		0		
Bit 26	SA		0		
Bit 27	SA		0		
Bit 28	SA	start address	0		0
Bit 29	SA		0		
Bit 30	SA		0		
Bit 31	SA		0	start address bit LSB	
LSB	name	description	value	selection	HEX

### Chip-0-Select-End-Address-Register

MSB	name	description	value	selection	HEX
Bit 0	Rsrvd	reserved	0		0
Bit 1	Rsrvd		0		
Bit 2	Rsrvd		0		
Bit 3	Rsrvd		0		
Bit 4	Rsrvd	reserved	0		0
Bit 5	Rsrvd		0		
Bit 6	Rsrvd		0		
Bit 7	Rsrvd		0		
Bit 8	Rsrvd	reserved	0		0
Bit 9	Rsrvd		0		
Bit 10	Rsrvd		0		
Bit 11	Rsrvd		0		
Bit 12	Rsrvd	reserved	0		0
Bit 13	Rsrvd		0		
Bit 14	Rsrvd		0		
Bit 15	Rsrvd		0		
Bit 16	EA	end address	1	end address bit MSB	F
Bit 17	EA		1		
Bit 18	EA		1		
Bit 19	EA		1		
Bit 20	EA	end address	1		C
Bit 21	EA		1		
Bit 22	EA		0		
Bit 23	EA		0		
Bit 24	EA	end address	1		F
Bit 25	EA		1		
Bit 26	EA		1		
Bit 27	EA		1		
Bit 28	EA	end address	1		F
Bit 29	EA		1		
Bit 30	EA		1		
Bit 31	EA		1	end address bit LSB	
LSB	name	description	value	selection	HEX

## Chip-Select-Configuration-Register-0

MSB	name	description	value	selection	HEX
Bit 0	WP	WaitP	0		0
Bit 1	WP		0		
Bit 2	WP		0		
Bit 3	WP		0		
Bit 4	WP	WaitP	0		0
Bit 5	WP		0		
Bit 6	WP		0		
Bit 7	WP		0		
Bit 8	WX	WaitX	0		0
Bit 9	WX		0		
Bit 10	WX		0		
Bit 11	WX		0		
Bit 12	WX	WaitX	0		2
Bit 13	WX		0		
Bit 14	WX		1	(2+2)*CLK=120ns	
Bit 15	WX		0		
Bit 16	MX	multiplexed mode	0		7
Bit 17	Rsrvd	reserved, must be 1	1		
Bit 18	AA	acknowledge active	1		
Bit 19	CE	CS pin enable	1		
Bit 20	AS	Address size	1	24 Bit	8
Bit 21	AS		0		
Bit 22	DS	Data size	0	8 Bit	
Bit 23	DS		0		
Bit 24	Bank	msb bank bit for AD26	0		0
Bit 25	Bank	lsb bank bit for AD25	0		
Bit 26	WTyp	waitstate type	0	WaitX for R & W	
Bit 27	WTyp	waitstate type	0		
Bit 28	WS	write swap bit	0	no swap	0
Bit 29	RS	read swap bit	0	no swap	
Bit 30	WO	write only	0	write allowed	
Bit 31	RO	read only	0	read allowed	
LSB	name	description	value	selection	HEX

## SRAM:

The static RAM of the MPX5200 consists of two devices and works in the 8 bit non-multiplexed mode with 24 address lines. The used devices are controlled via the select line CS1#, the LOE# and the LWE# line by the local bus of the MPC5200B. The data contents of the SRAM devices is protected by a local gold capacitor, which is also used to keep the onboard RTC running during short power down periods.

### ***SRAM Pin Configuration:***

MPC5200B Signal	Function	SRAM Signal
AD31-AD24	Data-Bus	D0-D7
AD31-AD24	Data-Bus	D8-D15
via CS1# + AD20 + logic	Chip Select	CE
LWE#	Write Enable	WE
LOE#	Read Enable	OE
via AD0 + logic	Byte Enable	LB/UB
AD1-AD19	Address-Bus	A0-A18

### Chip-1-Select-Start-Address-Register

MSB	name	description	value	selection	HEX
Bit 0	Rsrvd	reserved	0		0
Bit 1	Rsrvd		0		
Bit 2	Rsrvd		0		
Bit 3	Rsrvd		0		
Bit 4	Rsrvd	reserved	0		0
Bit 5	Rsrvd		0		
Bit 6	Rsrvd		0		
Bit 7	Rsrvd		0		
Bit 8	Rsrvd	reserved	0		0
Bit 9	Rsrvd		0		
Bit 10	Rsrvd		0		
Bit 11	Rsrvd		0		
Bit 12	Rsrvd	reserved	0		0
Bit 13	Rsrvd		0		
Bit 14	Rsrvd		0		
Bit 15	Rsrvd		0		
Bit 16	SA	start address	1	start address bit MSB	F
Bit 17	SA		1		
Bit 18	SA		1		
Bit 19	SA		1		
Bit 20	SA	start address	0		1
Bit 21	SA		0		
Bit 22	SA		0		
Bit 23	SA		1		
Bit 24	SA	start address	0		0
Bit 25	SA		0		
Bit 26	SA		0		
Bit 27	SA		0		
Bit 28	SA	start address	0		0
Bit 29	SA		0		
Bit 30	SA		0		
Bit 31	SA		0	start address bit LSB	
LSB	name	description	value	selection	HEX

### Chip-1-Select-End-Address-Register

MSB	name	description	value	selection	HEX
Bit 0	Rsrvd	reserved	0		0
Bit 1	Rsrvd		0		
Bit 2	Rsrvd		0		
Bit 3	Rsrvd		0		
Bit 4	Rsrvd	reserved	0		0
Bit 5	Rsrvd		0		
Bit 6	Rsrvd		0		
Bit 7	Rsrvd		0		
Bit 8	Rsrvd	reserved	0		0
Bit 9	Rsrvd		0		
Bit 10	Rsrvd		0		
Bit 11	Rsrvd		0		
Bit 12	Rsrvd	reserved	0		0
Bit 13	Rsrvd		0		
Bit 14	Rsrvd		0		
Bit 15	Rsrvd		0		
Bit 16	EA	end address	1	end address bit MSB	F
Bit 17	EA		1		
Bit 18	EA		1		
Bit 19	EA		1		
Bit 20	EA	end address	0		1
Bit 21	EA		0		
Bit 22	EA		0		
Bit 23	EA		1		
Bit 24	EA	end address	0		1
Bit 25	EA		0		
Bit 26	EA		0		
Bit 27	EA		1		
Bit 28	EA	end address	1		F
Bit 29	EA		1		
Bit 30	EA		1		
Bit 31	EA		1	end address bit LSB	
LSB	name	description	value	selection	HEX

## Chip-Select-Configuration-Register-1

MSB	name	description	value	selection	HEX
Bit 0	WP	WaitP	0		0
Bit 1	WP		0		
Bit 2	WP		0		
Bit 3	WP		0		
Bit 4	WP	WaitP	0		0
Bit 5	WP		0		
Bit 6	WP		0		
Bit 7	WP		0		
Bit 8	WX	WaitX	0		0
Bit 9	WX		0		
Bit 10	WX		0		
Bit 11	WX		0		
Bit 12	WX	WaitX	0		1
Bit 13	WX		0		
Bit 14	WX		0		
Bit 15	WX		1	(2+1)*CLK=90ns	
Bit 16	MX	multiplexed mode	0		7
Bit 17	Rsrvd	reserved, must be 1	1		
Bit 18	AA	acknowledge active	1		
Bit 19	CE	CS pin enable	1		
Bit 20	AS	Address size	1	24 Bit	8
Bit 21	AS		0		
Bit 22	DS	Data size	0	8 Bit	
Bit 23	DS		0		
Bit 24	Bank	msb bank bit for AD26	0		0
Bit 25	Bank	lsb bank bit for AD25	0		
Bit 26	WTyp	waitstate type	0	WaitX for R & W	
Bit 27	WTyp	waitstate type	0		
Bit 28	WS	write swap bit	0	no swap	0
Bit 29	RS	read swap bit	0	no swap	
Bit 30	WO	write only	0	write allowed	
Bit 31	RO	read only	0	read allowed	
LSB	name	description	value	selection	HEX

## DiskOnChip:

There is a DiskOnChip device onboard of the MPX5200. It consists of a single device and works in the 8 bit non-multiplexed mode with 24 address lines . The used device MD8832-d1G-V3XP from M-SYSTEMS is controlled via select line CS2# , the LOE# and the LWE# line by the local bus of the MPC5200B. Optional the IRQ line of the device can be connected to IRQ3# via soldering link R8.

### ***DiskOnChip Pin Configuration:***

MPC5200B Signal	Function	DiskOnChip Signal
	Data-Bus	not connected
AD31 – AD24	Data-Bus	D7 - D0
LCS2#	Chip Select	CE
LWE#	Write Enable	WE
LOE#	Read Enable	OE
PCICLK0	Clock	CLK
AD12-AD0	Address-Bus	A0-A12
IRQ3#	Interrupt	IRQ connected to IRQ3# via R8
HRST#	Reset	RST
---	not used	DRQ tied to high
---	not used	DBSY tied to high
---	not used	LCK tied to high
---	8 bit mode	CFG tied to low
---	single chip 1	ID0 tied to low
---	non-mux-mode	ID1 tied to low

## Chip-2-Select-Start-Address-Register

MSB	name	description	value	selection	HEX
Bit 0	Rsrvd	reserved	0		0
Bit 1	Rsrvd		0		
Bit 2	Rsrvd		0		
Bit 3	Rsrvd		0		
Bit 4	Rsrvd	reserved	0		0
Bit 5	Rsrvd		0		
Bit 6	Rsrvd		0		
Bit 7	Rsrvd		0		
Bit 8	Rsrvd	reserved	0		0
Bit 9	Rsrvd		0		
Bit 10	Rsrvd		0		
Bit 11	Rsrvd		0		
Bit 12	Rsrvd	reserved	0		0
Bit 13	Rsrvd		0		
Bit 14	Rsrvd		0		
Bit 15	Rsrvd		0		
Bit 16	SA	start address	1	start address bit MSB	E
Bit 17	SA		1		
Bit 18	SA		1		
Bit 19	SA		0		
Bit 20	SA	start address	0		0
Bit 21	SA		0		
Bit 22	SA		0		
Bit 23	SA		0		
Bit 24	SA	start address	0		0
Bit 25	SA		0		
Bit 26	SA		0		
Bit 27	SA		0		
Bit 28	SA	start address	0		0
Bit 29	SA		0		
Bit 30	SA		0		
Bit 31	SA		0	start address bit LSB	
LSB	name	description	value	selection	HEX

## Chip-2-Select-End-Address-Register

MSB	name	description	value	selection	HEX
Bit 0	Rsrvd	reserved	0		0
Bit 1	Rsrvd		0		
Bit 2	Rsrvd		0		
Bit 3	Rsrvd		0		
Bit 4	Rsrvd	reserved	0		0
Bit 5	Rsrvd		0		
Bit 6	Rsrvd		0		
Bit 7	Rsrvd		0		
Bit 8	Rsrvd	reserved	0		0
Bit 9	Rsrvd		0		
Bit 10	Rsrvd		0		
Bit 11	Rsrvd		0		
Bit 12	Rsrvd	reserved	0		0
Bit 13	Rsrvd		0		
Bit 14	Rsrvd		0		
Bit 15	Rsrvd		0		
Bit 16	EA	end address	1	end address bit MSB	E
Bit 17	EA		1		
Bit 18	EA		1		
Bit 19	EA		0		
Bit 20	EA	end address	0		0
Bit 21	EA		0		
Bit 22	EA		0		
Bit 23	EA		0		
Bit 24	EA	end address	0		0
Bit 25	EA		0		
Bit 26	EA		0		
Bit 27	EA		0		
Bit 28	EA	end address	1		F
Bit 29	EA		1		
Bit 30	EA		1		
Bit 31	EA		1	end address bit LSB	
LSB	name	description	value	selection	HEX

## Chip-Select-Configuration-Register-2

MSB	name	description	value	selection	HEX
Bit 0	WP	WaitP	0		0
Bit 1	WP		0		
Bit 2	WP		0		
Bit 3	WP		0		
Bit 4	WP	WaitP	0		0
Bit 5	WP		0		
Bit 6	WP		0		
Bit 7	WP		0		
Bit 8	WX	WaitX	0		0
Bit 9	WX		0		
Bit 10	WX		0		
Bit 11	WX		0		
Bit 12	WX	WaitX	0		2
Bit 13	WX		0		
Bit 14	WX		1	(2+2)*CLK=120ns	
Bit 15	WX		0		
Bit 16	MX	multiplexed mode	0		7
Bit 17	Rsrvd	reserved, must be 1	1		
Bit 18	AA	acknowledge active	1		
Bit 19	CE	CS pin enable	1		
Bit 20	AS	Address size	1	24 Bit	8
Bit 21	AS		0		
Bit 22	DS	Data size	0	8 Bit	
Bit 23	DS		0		
Bit 24	Bank	msb bank bit for AD26	0		0
Bit 25	Bank	lsb bank bit for AD25	0		
Bit 26	WTyp	waitstate type	0	WaitX for R & W	
Bit 27	WTyp	waitstate type	0		
Bit 28	WS	write swap bit	0	no swap	0
Bit 29	RS	read swap bit	0	no swap	
Bit 30	WO	write only	0	write allowed	
Bit 31	RO	read only	0	read allowed	
LSB	name	description	value	selection	HEX

## I2C EEPROM:

### **EEPROM I2C Access Address:**

Device:	Hex:	binary I <sup>2</sup> C address							read/write
AT24C128	A6/A7	1	0	1	0	0	1	1	1/0

The AT24C128 uses a two 8 bit address words following the shown device address for data access. The write protect function of the Atmel EEPROM device is disabled.

## Real Time Clock PCF8563T:

### **RTC I2C Access Address:**

Device:	Hex:	binary I <sup>2</sup> C address							read/write
PCF8563T	A2/A3	1	0	1	0	0	0	1	1/0

The PCF8563T uses an 8 bit address word following the shown device address for register and data access. The interrupt line of the RTC is not connected.

## RTC Address Map:

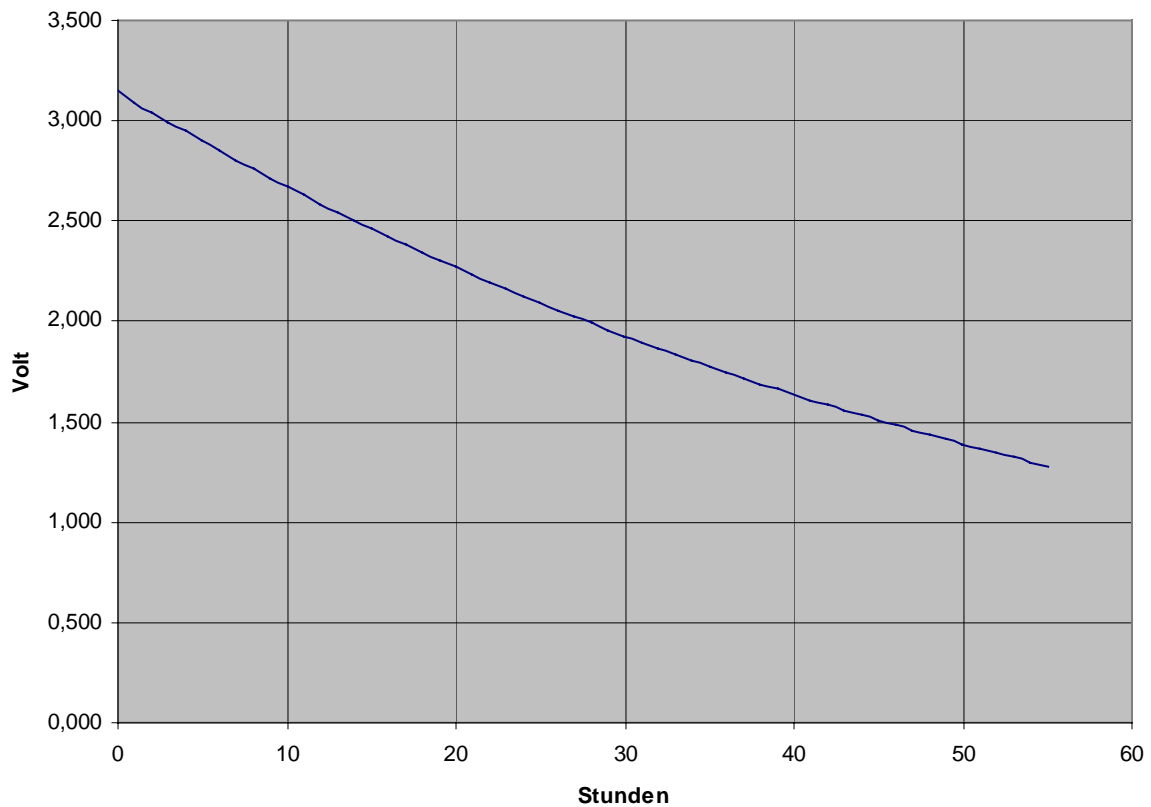
bit oriented registers									
address	register name	D7	D6	D5	D4	D3	D2	D1	D0
\$00	Control/Status 1	TEST 1	0	STOP	0	TEST C	0	0	0
\$01	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
\$0D	CLKOUT frequency	FE	--	--	--	--	--	FD1	FD0
\$0E	Timer control	TE	--	--	--	--	--	TD1	TD0
\$0F	Timer countdown value	<timer countdown value>							

BCD formatted registers									
address	register name	D7	D6	D5	D4	D3	D2	D1	D0
		BCD format tens nibble				BCD format units nibble			
\$02	Seconds	VL	<seconds 00 to 59 coded in BCD>						
\$03	Minutes	--	<minutes 00 to 59 coded in BCD>						
\$04	Hours	--	--	<hours 00 to 23 coded in BCD>					
\$05	Days	--	--	<days 01 to 31 coded in BCD>					
\$06	Weekdays	--	--	--	--	--	<weekday 0 to 6>		
\$07	Month/Century	C	--	--	<month 01 to 12 coded in BCD>				
\$08	Years	<years 00 to 99 coded in BCD>							
\$09	Minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
\$0A	Hour alarm	AE	--	<hour alarm 00 to 23 coded in BCD>					
\$0B	Day alarm	AE	--	<day alarm 01 to 31 coded in BCD>					
\$0C	Weekday alarm	AE	--	--	--	--	<weekday alarm 0 to 6>		

## Data Retention

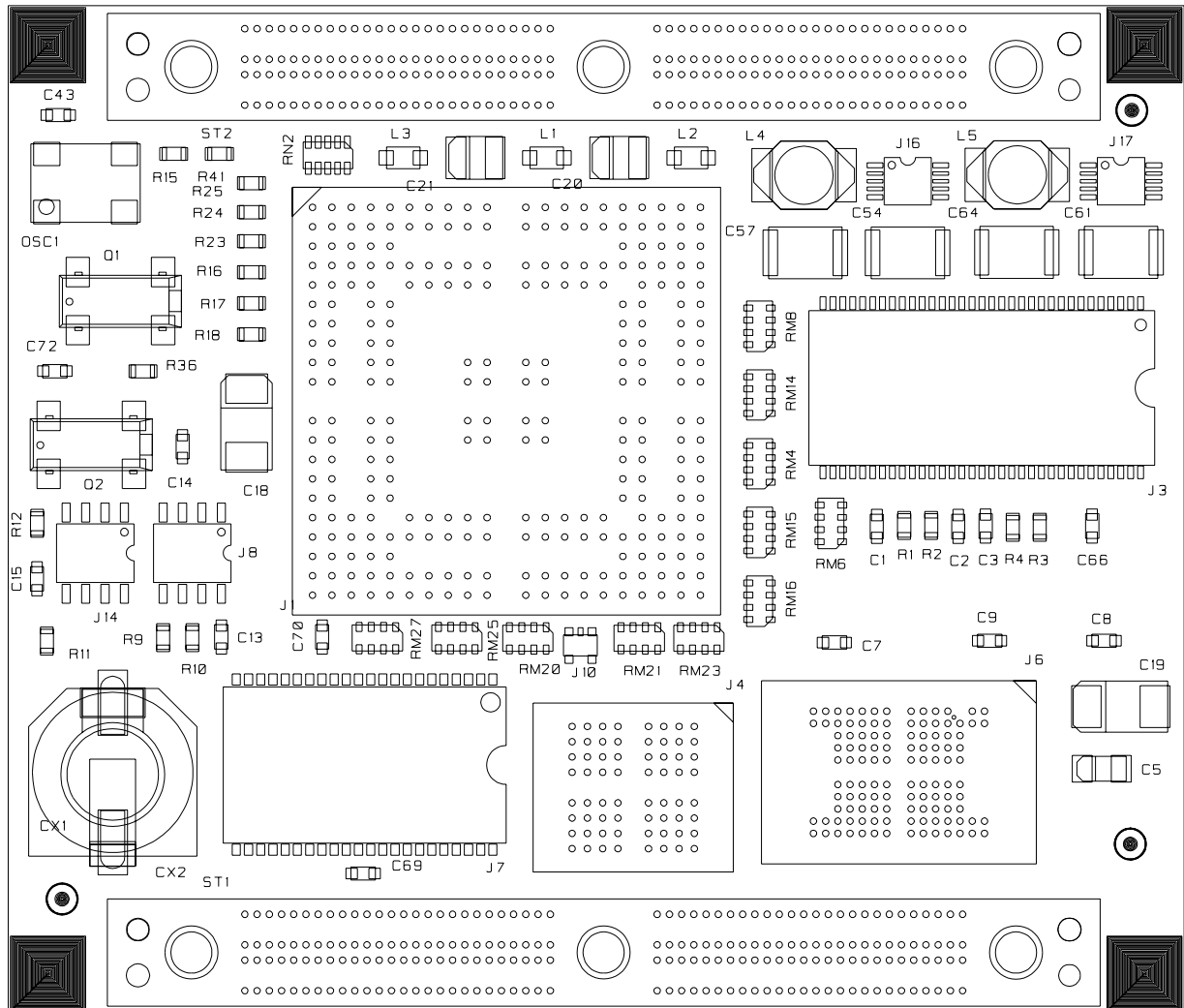
The primary data retention is performed by a local gold capacitor. Additional backup power can be supplied via signal STDBY on connector ST2-c39. The external supply voltage must not exceed 3.3V. The RTC PCF8563T works with a minimum supply voltage of 1.0 volts, while the SRAM devices needs at least 1.5 volts for data retention. The CLKOUT and timer of the PCF8563T should be disabled to reduce power consumption.

### Capacitor Backup Time

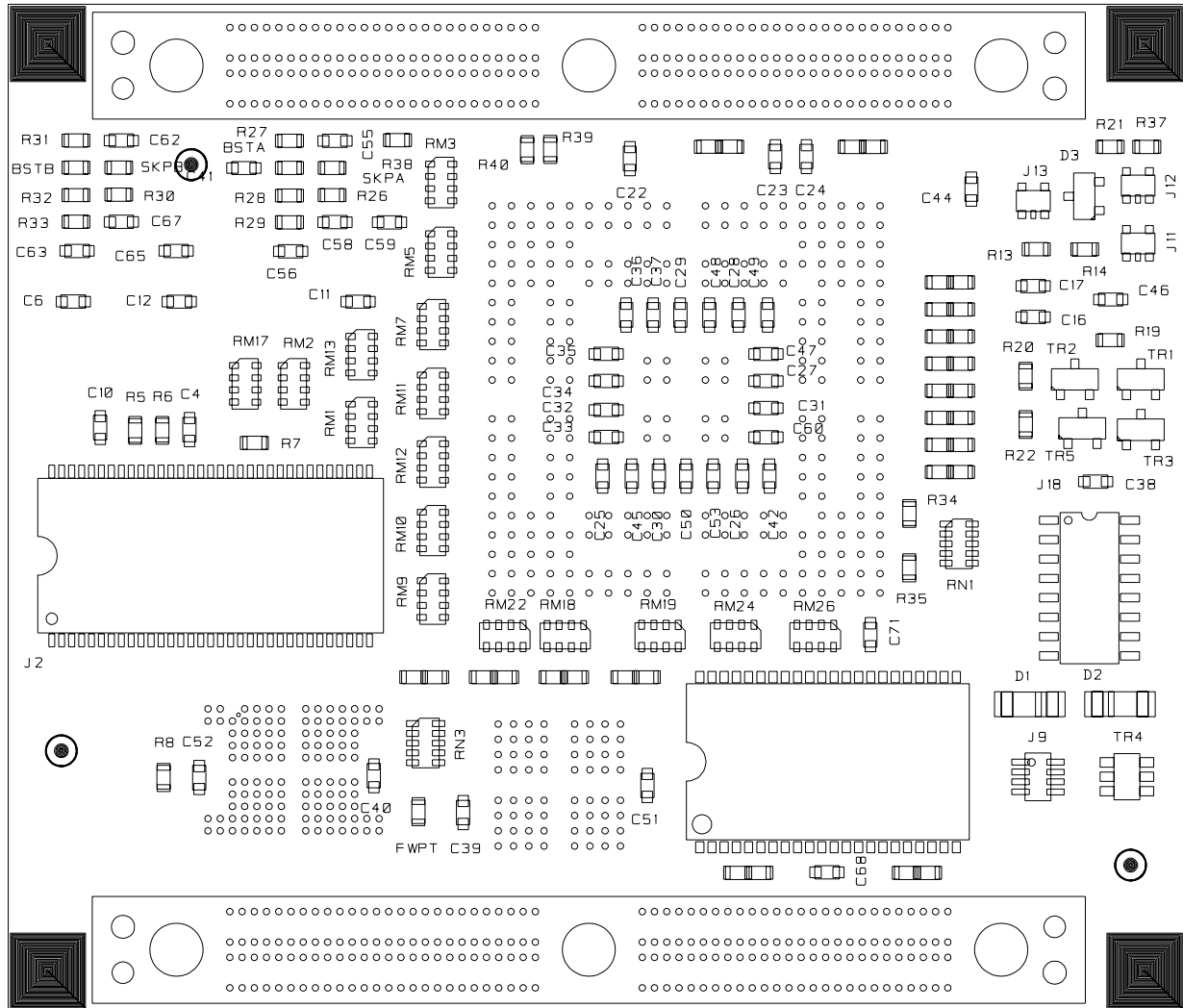


## Appendices

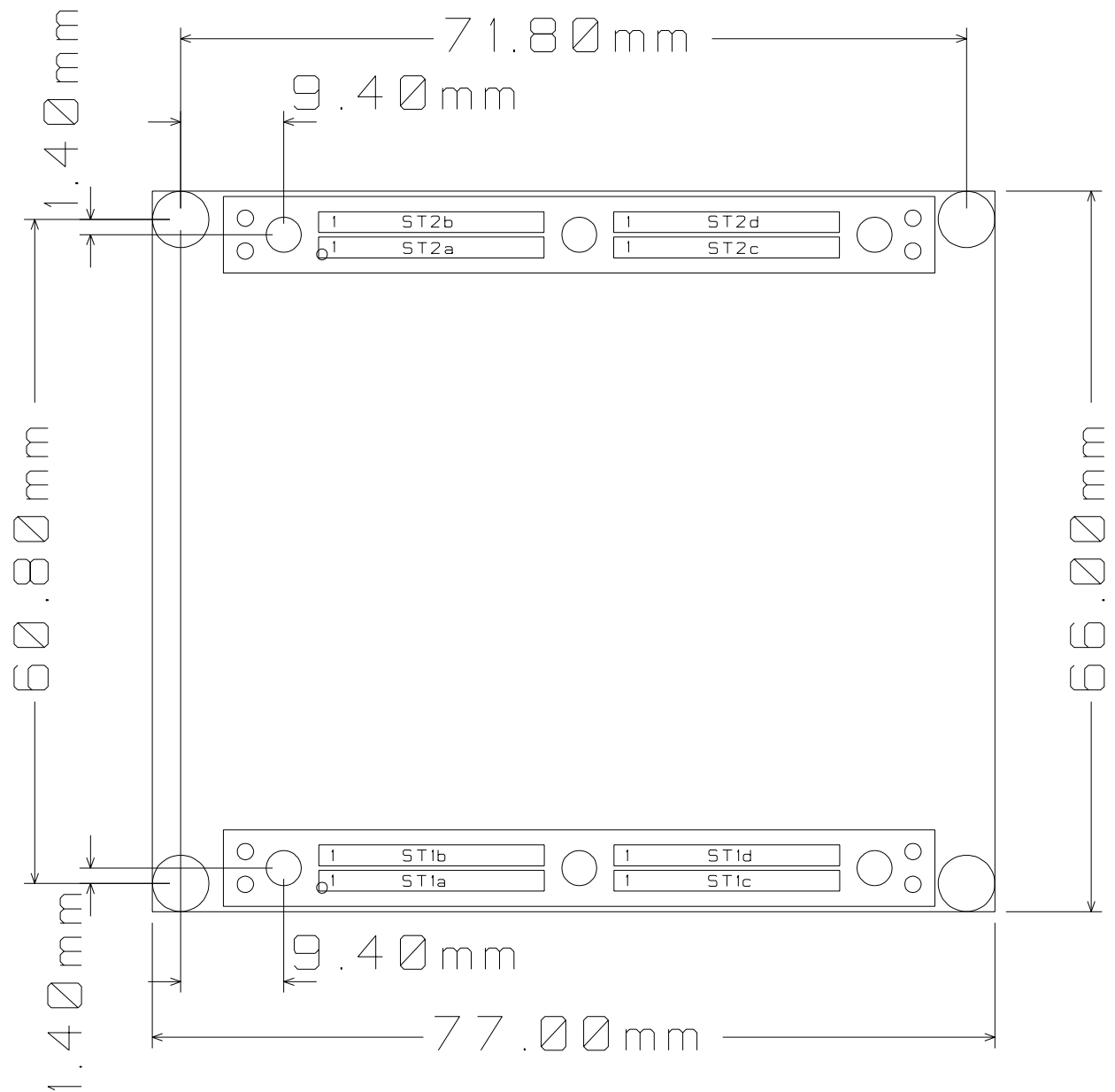
# Layout Component Side



# Layout Solder Side



## Physical Dimensions (Top View)



## **Schematics MPX5200 (please contact *MicroSys*)**