

# **Microsys**

**User's Manual**

**MPX2020 Rev. 2**

**1<sup>st</sup> edition**

# Declaration of Conformity

We, Manufacturer  
MicroSys Electronics GmbH  
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D-82054 Sauerlach  
Germany

Declare that the product

**MPX2020**

is in conformity with:

**EN 50081-1 Generic Emission Standard**  
**EN 50082-1 Generic Immunity Standard**

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above-mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position:       General Manager

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## Edition

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## Table of Contents

1. CHIP SELECT OVERVIEW .....	7
2. ADDRESS MAP .....	7
3. I <sup>2</sup> C-1 ADDRESS OVERVIEW .....	8
4. I <sup>2</sup> C-2 ADDRESS OVERVIEW .....	8
5. POWER SUPPLY RATINGS .....	9
6. I/O SUPPLY RATINGS .....	10
7. BACKUP SUPPLY RATINGS .....	11
7.1. CAPACITOR BACKUP TIME AT FULL TEMPERATURE RANGE .....	11
8. THE P2020 QORIQ PROCESSOR .....	12
9. BDM JTAG PORT CONNECTION .....	12
10. INTERRUPT CONFIGURATION .....	13
11. LOCAL BUS .....	14
11.1. LOCAL BUS PIN CONFIGURATION .....	14
12. SERDES ST1-CONNECTOR PINOUT .....	15
13. MII INTERFACE ST1-CONNECTOR PINOUT .....	16
14. LOCAL BUS ST2-CONNECTOR PINOUT .....	17
15. I/O INTERFACE ST2-CONNECTOR PINOUT: .....	18
16. DDR-II SDRAM MEMORY .....	19
16.1. MEMORY BUS PIN CONFIGURATION .....	19
16.2. DDR SDRAM CS0-BNDS REGISTER .....	20
16.3. DDR SDRAM CS0-CONFIG REGISTER .....	21
16.4. DDR-SDRAM-CS0-CFG2 REGISTER .....	22
16.5. DDR SDRAM CS1-BNDS REGISTER .....	23
16.6. DDR SDRAM CS1-CONFIG REGISTER .....	24
16.7. DDR-SDRAM-CS1-CFG2 REGISTER .....	25
16.8. DDR-SDRAM-CFG1 REGISTER .....	26
16.9. DDR-SDRAM-CFG2 REGISTER .....	27
16.10. DDR-SDRAM-MODE-2 REGISTER .....	28
16.11. DDR-SDRAM-MD-CNTL REGISTER .....	29
16.12. DDR SDRAM TIMING-CFG-0 REGISTER .....	30
16.13. DDR SDRAM TIMING-CFG-1 REGISTER .....	31
16.14. DDR SDRAM TIMING-CFG-2 REGISTER .....	32
16.15. DDR SDRAM TIMING-CFG-3 REGISTER .....	33
16.16. DDR-SDRAM-INTERVAL REGISTER .....	34
16.17. DDR-SDRAM-MODE REGISTER .....	35
17. NAND FLASH MEMORY .....	36
17.1. NAND FLASH PIN CONFIGURATION .....	36
17.2. BR0 BASE REGISTER .....	37
17.3. OR0 OPTION REGISTER .....	38
18. I <sup>2</sup> C TEMPERATURE SENSOR .....	39
18.1. TEMPERATURE SENSOR I <sup>2</sup> C ACCESS ADDRESS .....	39
19. I <sup>2</sup> C EEPROM-I .....	40
19.1. EEPROM-I I <sup>2</sup> C ACCESS ADDRESS .....	40
20. I <sup>2</sup> C EEPROM-II .....	40
20.1. EEPROM-II I <sup>2</sup> C ACCESS ADDRESS .....	40
21. I <sup>2</sup> C REAL TIME CLOCK .....	41
21.1. RTC I <sup>2</sup> C ACCESS ADDRESSES .....	41

21.2. RTC GOLD CAP BACKUP TIME @25°C..... 41  
21.3. RTC ADDRESS MAP ..... 42  
22. HARDWARE WATCHDOG TIMER ..... 43

## 1. Chip Select Overview

<b>Signal</b>	<b>Function</b>	<b>Bus width</b>	<b>Mode</b>	<b>Size</b>	<b>Description</b>
MCS0	SDRAM	64Bit	DDR-II	1GByte	ECC support
MCS1	SDRAM	64Bit	DDR-II	1GByte	ECC support
MCS2	not used	---	---	---	not connected
MCS3	not used	---	---	---	not connected
LCS0	FLASH	8 Bit	NAND	256 MByte	connected to ST1.b14
LCS1	not used onboard	---	---	---	connected to ST1.b16
LCS2	not used onboard	---	---	---	connected to ST1.b18
LCS3	not used onboard	---	---	---	connected to ST1.b20
LCS4	not used onboard	---	---	---	connected to ST1.b22
LCS5	not used onboard	---	---	---	connected to ST1.b28
LCS6	not used onboard	---	---	---	connected to ST1.b30
LCS7	not used onboard	---	---	---	connected to ST1.b32

## 2. Address map

<b>Type</b>	<b>Base</b>	<b>End</b>	<b>Select</b>	<b>Size</b>
CCSRBAR	\$0 E000 0000	\$0 E00F FFFF		
DDR-II SDRAM	\$0 0000 0000	\$0 xxxx FFFF	MCS0	64Bit
DDR-II SDRAM	\$0 xxxx 0000	\$0 xFFF FFFF	MCS1	64Bit
NAND-Flash	\$0 FE00 0000	\$0 FFFF FFFF	LCS0	8Bit
not initialized			LCS1	
not initialized			LCS2	
not initialized			LCS3	
not initialized			LCS4	
not initialized			LCS5	
not initialized			LCS6	
not initialized			LCS7	

### 3. I<sup>2</sup>C-1 Address Overview

<i>Device</i>	<i>Hex</i>	<i>7 bit binary I<sup>2</sup>C address</i>							<i>read/write</i>
DS75LV	0x4F	1	0	0	1	1	1	1	1/0
AT24C128	0x50	1	0	1	0	0	0	0	1/0
AT24C128	0x52	1	0	1	0	0	1	0	1/0
ISL12020	0x57	1	0	1	0	1	1	1	1/0
	0x6F	1	1	0	1	1	1	1	1/0

### 4. I<sup>2</sup>C-2 Address Overview

<i>Device</i>	<i>Hex</i>	<i>7 bit binary I<sup>2</sup>C address</i>							<i>read/write</i>
									1/0
									1/0

## 5. Power Supply Ratings

The MPX2020 module must be supplied with single 3.3V. There are two 12 pin wide VDD supply blocks on the connectors ST1-A and ST2-C and several GND pins distributed over connector ST1 and ST2. For a proper operation, all ground pins and all VDD pins should be connected to the carrier board.

<b>3.3V</b>	<b>ST1-A</b>
VDD	pin a15
VDD	pin a17
VDD	pin a19
VDD	pin a21
VDD	pin a23
VDD	pin a25
VDD	pin a27
VDD	pin a29
VDD	pin a31
VDD	pin a33
VDD	pin a35
VDD	pin a37

<b>3.3V</b>	<b>ST2-C</b>	<b>ST2-C</b>	<b>3.3V</b>
VDD	pin c41	pin c42	VDD
VDD	pin c43	pin c44	VDD
VDD	pin c45	pin c46	VDD
VDD	pin c47	pin c48	VDD
VDD	pin c49	pin c50	VDD
VDD	pin c51	pin c52	VDD

<b>Name</b>	<b>Rating</b>	<b>Current</b>	<b>Tolerance</b>	<b>Ripple</b>
VDD	+3.3VDC	peak xA	+/-5%	max.50mV

## 6. I/O Supply Ratings

The signal groups for TSEC, LBC, GPIO, eSDHC, SPI and USB can work with different I/O voltages. These signals are split into 3 groups, which can be supplied onboard or by external supply pins. If the according control pins are left open or tied to ground, the I/O supplies are connected to the local 3.3V source. If these pins are tied to 3.3V, an external supply voltage within the given range must be connected to the according supply pins. If the applied I/O voltage exceeds the configured value, irreversible device damage may occur.

<b>Group</b>	<b>Operation</b>	<b>Control</b>	<b>Supply</b>	<b>Signals</b>
TSEC	3.3V/2.5V	LVSEL	LVDD	all MII signals
LBC	3.3V/2.5V/1.8V	BVSL0/1	BVDD	LBC / GPIO
USB	3.3V/2.5V/1.8V	UVSL0/1	UVDD	USB / eSDHC / SPI

<b>TSEC</b>		<b>2.5V external operation</b>	<b>3.3V internal operation</b>
LVDD	ST1.c2	supply with 2.5V +/-5%	leave open
LVDD	ST1.c4	supply with 2.5V +/-5%	leave open
LVSEL	ST1.c6	tie to 3.3V	leave open or tie to ground

<b>LBC</b>		<b>1.8V external</b>	<b>2.5V external</b>	<b>3.3V internal</b>
BVDD	ST2.b2	supply with 1.8V +/-5%	supply with 2.5V +/-5%	leave open
BVDD	ST2.b4	supply with 1.8V +/-5%	supply with 2.5V +/-5%	leave open
BVSL0	ST2.b6	tie to 3.3V	open or tie to ground	open or tie to ground
BVSL1	ST2.b8	open or tie to ground	tie to 3.3V	open or tie to ground

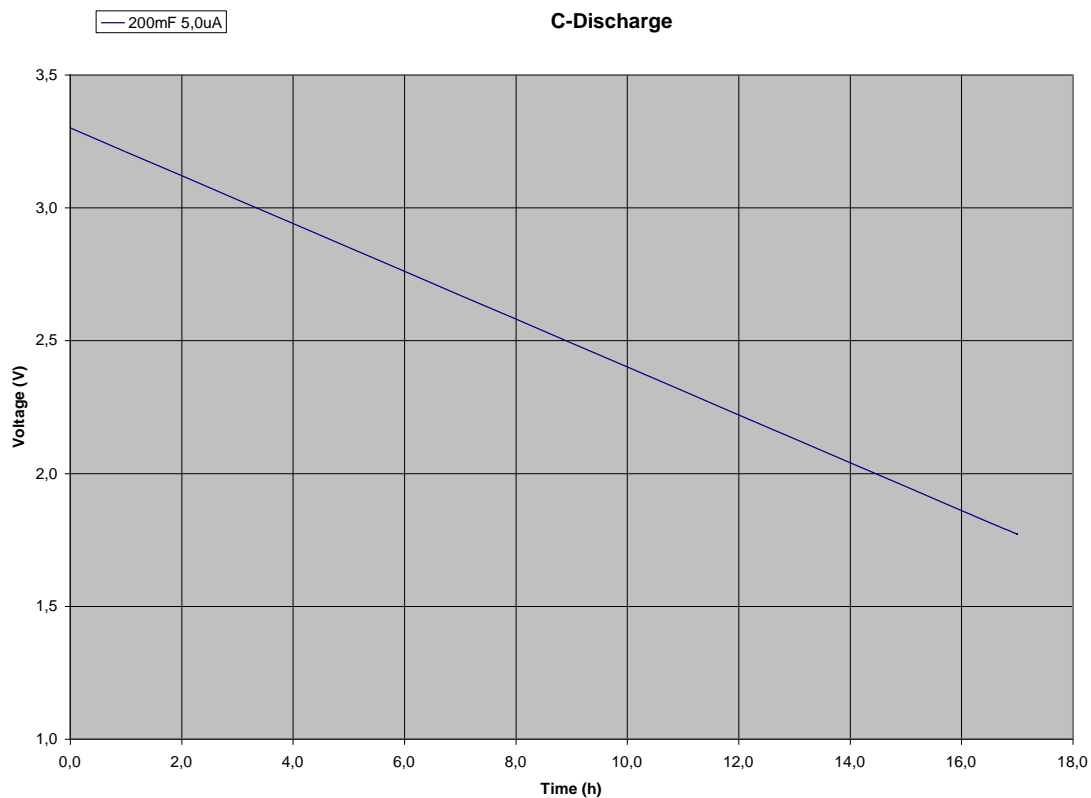
<b>USB</b>		<b>1.8V external</b>	<b>2.5V external</b>	<b>3.3V internal</b>
UVDD	ST2.b52	supply with 1.8V +/-5%	supply with 2.5V +/-5%	leave open
UVDD	ST2.b50	supply with 1.8V +/-5%	supply with 2.5V +/-5%	leave open
UVSL0	ST2.b46	tie to 3.3V	open or tie to ground	open or tie to ground
UVSL1	ST2.b48	open or tie to ground	tie to 3.3V	open or tie to ground

## 7. Backup Supply Ratings

The MPX2020 contains a real-time clock with an automatic backup feature supported by the onboard gold capacitor. For extended backup times an external power can be supplied via the STDBY line.

<b>Signal</b>	<b>Pin</b>	<b>Rating</b>	<b>Current</b>	<b>Ripple</b>
STDBY	ST2.c39	+1.8V to +3.3V	max. 5uA	max.50mV

### 7.1. Capacitor Backup Time at full Temperature Range



## 8. The P2020 QorIQ Processor

The P2020 QorIQ CPU is connected to a 64+8 bit wide DDR-II SDRAM with ECC memory protection. The local bus side handles the onboard NAND Flash device by the select line LCS0. The select lines LCS1 to LCS7 can be used for other purposes. The I<sup>2</sup>C port 1 of the processor is connected to four local devices, which respond on five I<sup>2</sup>C addresses. The I<sup>2</sup>C port 2 is not connected to any local devices.

## 9. BDM JTAG Port Connection

The JTAG/COP port of the P2020 can be accessed via ST2-A by the following signals:

<i>Description</i>	<i>Signal</i>	<i>ST2</i>	<i>ST2</i>	<i>Signal</i>	<i>Description</i>
	TMS	pin a39	pin a40	CKSTI	4k7 to VDD
	TDI	pin a41	pin a42	CKSTO	4k7 to VDD
	TDO	pin a43	pin a44		
4k7 to VDD	TCK	pin a45	pin a46	HRST#	4k7 to VDD
4k7 to GND	TRST#	pin a47	pin a48	SRST#	4k7 to VDD
	GND	pin a49	pin a50	SCMODE	4k7 to VDD
	GND	pin a51	pin a52		

## 10. Interrupt Configuration

<i>P2020 Signal</i>	<i>Destination</i>	<i>onboard source</i>
IRQ0#	ST2-b39	RTC ISL12020 via link RIRQ
IRQ1#	ST2-b41	---
IRQ2#	ST2-b43	---
IRQ3#	ST2-b45	---
IRQ4#	ST2-b47	---
IRQ5#	ST2-b40	---
IRQ6#	ST2-b42	---

## 11. Local Bus

The local bus of the MPX2020 is accessible via the connectors ST2-A and ST2-B. Besides the LCLK1 signal, all local bus lines are connected, even if onboard devices use some of them.

### 11.1. Local Bus Pin Configuration

<b>P2020 Signal</b>	<b>Destination</b>	<b>onboard function</b>
LAD(15:0)	ST2-A	Address/Data Bus
LA(31:16)	ST2-A	Address Bus
LA16	ST2-a21	not used, PLD controlled configuration line
LA18	ST2-a25	not used, PLD controlled configuration line
LA19	ST2-a27	not used, PLD controlled configuration line
LA23	ST2-a35	not used, pulldown for configuration
LA24	ST2-a22	not used, pulldown for configuration
LA25	ST2-a24	not used, pulldown for configuration
LA26	ST2-a26	not used, pulldown for configuration
LA27	ST2-a28	not used, PLD controlled configuration line
LA29	ST2-a32	not used, pullup/pulldown for configuration
LA30	ST2-a34	not used, pullup/pulldown for configuration
LA31	ST2-a36	not used, pullup/pulldown for configuration
LCSE	ST2-c40	enable NAND Flash Chip Select, 1K0 pulldown to GND
LCS0#	ST2-b14	NAND Flash Chip Select
LCS1#	ST2-b16	not used, 4k7 pullup to VDD
LCS2#	ST2-b18	not used, 4k7 pullup to VDD
LCS3#	ST2-b20	not used, 4k7 pullup to VDD
LCS4#	ST2-b22	not used, 4k7 pullup to VDD
LCS5# / DREQ2#	ST2-b28	not used, 4k7 pullup to VDD
LCS6# / DACK2#	ST2-b30	not used
LCS7# / DONE2#	ST2-b32	not used
LGPL0	ST2-b11	NAND Flash CLE, 4k7 pullup to VDD
LGPL1	ST2-b13	NAND Flash ALE, PLD controlled configuration line
LGPL2	ST2-b15	NAND Flash RE, pullup/pulldown for configuration
LGPL3	ST2-b17	not used, PLD controlled configuration line
LGPL4	ST2-b19	not used, 4k7 pullup to VDD
LGPL5	ST2-b21	not used, PLD controlled configuration line
LALE	ST2-b9	not used, pullup/pulldown for configuration
LBCTL	ST2-b23	not used, pullup/pulldown for configuration
LWE0#	ST2-b10	NAND Flash WE, pullup/pulldown for configuration
LWE1#	ST2-b12	not used, PLD controlled configuration line
LDP0	ST2-b5	not used, 4k7 pulldown to GND
LDP1	ST2-b7	not used, 4k7 pulldown to GND
LCLK0	ST2-b25	not used
LCLK1	----	not used
DREQ0#	ST2-b27	not used, 4k7 pullup to VDD
DACK0#	ST2-b29	not used
DONE0#	ST2-b31	not used
DREQ1#	ST2-b33	not used, 4k7 pullup to VDD
DACK1#	ST2-b35	not used
DONE1#	ST2-b37	not used
FLWP#	ST2-b38	NAND Flash & EEPROM-2 write protect, 4k7 to GND

## 12. Serdes ST1-Connector Pinout

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

	a1	a2	
	a3	a4	
	a5	a6	
PCIE-RXND	a7	a8	GND
PCIE-RXPD	a9	a10	GND
PCIE-TXND	a11	a12	PCIE-CLK3P
PCIE-TXPD	a13	a14	PCIE-CLK3N
VDD	a15	a16	GND
VDD	a17	a18	GND
VDD	a19	a20	GND
VDD	a21	a22	GND
VDD	a23	a24	GND
VDD	a25	a26	GND
VDD	a27	a28	GND
VDD	a29	a30	GND
VDD	a31	a32	GND
VDD	a33	a34	GND
VDD	a35	a36	GND
VDD	a37	a38	GND
PCIE-RXNC	a39	a40	PCIE-CLK0P
PCIE-RXPC	a41	a42	PCIE-CLK0N
PCIE-TXNC	a43	a44	GND
PCIE-TXPC	a45	a46	GND
	a47	a48	
	a49	a50	
	a51	a52	

GND	b1	b2	
GND	b3	b4	
	b5	b6	
	b7	b8	
	b9	b10	
	b11	b12	
	b13	b14	
	b15	b16	
GND	b17	b18	PCIE-RXNA
GND	b19	b20	PCIE-RXPA
PCIE-CLK2P	b21	b22	PCIE-TXNA
PCIE-CLK2N	b23	b24	PCIE-TXPA
PCFG0	b25	b26	GND
PCFG1	b27	b28	GND
PCIE-CLK1P	b29	b30	PCIE-RXNB
PCIE-CLK1N	b31	b32	PCIE-RXPB
GND	b33	b34	PCIE-TXNB
GND	b35	b36	PCIE-TXPB
	b37	b38	
	b39	b40	
	b41	b42	
	b43	b44	
	b45	b46	
	b47	b48	
GND	b49	b50	
GND	b51	b52	

### 13. MII Interface ST1-Connector Pinout

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

GND	c1	c2	LVDD
GND	c3	c4	LVDD
	c5	c6	LVSEL
ALRO1-1588	c7	c8	ALRO2-1588
PLSO1-1588	c9	c10	PLSO2-1588
MII1-RXER	c11	c12	
MII1-RXDV	c13	c14	MII1-TXER
MII1-COL	c15	c16	MII1-TXEN
MII1-CRS	c17	c18	MII1-RXD0
MII1-RXD7	c19	c20	MII1-RXD1
MII1-RXD6	c21	c22	MII1-RXD2
MII1-RXD5	c23	c24	MII1-RXD3
MII1-RXD4	c25	c26	MII1-RXCK
MII1-GTCK	c27	c28	GND
MII1-GXCK	c29	c30	GND
MII1-TXD4	c31	c32	MII1-TXCK
MII1-TXD5	c33	c34	MII1-TXD3
MII1-TXD6	c35	c36	MII1-TXD2
MII1-TXD7	c37	c38	MII1-TXD1
	c39	c40	MII1-TXD0
GPIO0	c41	c42	
GPIO1	c43	c44	
GPIO2	c45	c46	GPIO4
GPIO3	c47	c48	GPIO5
GND	c49	c50	GPIO6
GND	c51	c52	GPIO7

GND	d1	d2	MII-MDCK
GND	d3	d4	MII-MDIO
	d5	d6	MCFG
TRGI1-1588	d7	d8	TRGI2-1588
CLKI-1588	d9	d10	CLKO-1588
MII2-RXER	d11	d12	
MII2-RXDV	d13	d14	MII2-TXER
MII2-COL	d15	d16	MII2-TXEN
MII2-CRS	d17	d18	MII2-RXD0
MII2-RXD7	d19	d20	MII2-RXD1
MII2-RXD6	d21	d22	MII2-RXD2
MII2-RXD5	d23	d24	MII2-RXD3
MII2-RXD4	d25	d26	MII2-RXCK
	d27	d28	GND
MII2-GXCK	d29	d30	GND
MII2-TXD4	d31	d32	MII2-TXCK
MII2-TXD5	d33	d34	MII2-TXD3
MII2-TXD6	d35	d36	MII2-TXD2
MII2-TXD7	d37	d38	MII2-TXD1
	d39	d40	MII2-TXD0
GPIO8	d41	d42	
GPIO9	d43	d44	
GPIO10	d45	d46	GPIO12
GPIO11	d47	d48	GPIO13
GND	d49	d50	GPIO14
GND	d51	d52	GPIO15

## 14. Local Bus ST2-Connector Pinout

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

GND	a1	a2	LAD8
GND	a3	a4	LAD9
LAD0	a5	a6	LAD10
LAD1	a7	a8	LAD11
LAD2	a9	a10	LAD12
LAD3	a11	a12	LAD13
LAD4	a13	a14	LAD14
LAD5	a15	a16	LAD15
LAD6	a17	a18	GND
LAD7	a19	a20	GND
LA16	a21	a22	LA24
LA17	a23	a24	LA25
LA18	a25	a26	LA26
LA19	a27	a28	LA27
LA20	a29	a30	LA28
LA21	a31	a32	LA29
LA22	a33	a34	LA30
LA23	a35	a36	LA31
	a37	a38	
TMS	a39	a40	CKSTI
TDI	a41	a42	CKSTO
TDO	a43	a44	KRST#
TCK	a45	a46	HRST#
TRST#	a47	a48	SRST#
GND	a49	a50	SCMODE#
GND	a51	a52	LCFG

GND	b1	b2	BVDD
GND	b3	b4	BVDD
LDP0	b5	b6	BVSEL0
LDP1	b7	b8	BVSEL1
LALE	b9	b10	LWE0#
LGPL0	b11	b12	LWE1#
LGPL1	b13	b14	LCS0#
LGPL2	b15	b16	LCS1#
LGPL3	b17	b18	LCS2#
LGPL4	b19	b20	LCS3#
LGPL5	b21	b22	LCS4#
LBCTL	b23	b24	GND
LCLK0	b25	b26	GND
DREQ0#	b27	b28	DREQ2#
DACK0#	b29	b30	DACK2#
DONE0#	b31	b32	DONE2#
DREQ1#	b33	b34	
DACK1#	b35	b36	BMOD
DONE1#	b37	b38	FLWP#
IRQ0#	b39	b40	IRQ5#
IRQ1#	b41	b42	IRQ6#
IRQ2#	b43	b44	CSWDG#
IRQ3#	b45	b46	USSL0
IRQ4#	b47	b48	UVSL1
GND	b49	b50	UVDD
GND	b51	b52	UVDD

grey shaded: onboard pullup or pulldown resistors.

## 15. I/O Interface ST2-Connector Pinout:

Physical location:

c52	ST1	c1	a52	ST1	a1
d52	ST1	d1	b52	ST1	b1
c52	ST2	c1	a52	ST2	a1
d52	ST2	d1	b52	ST2	b1

<b>GND</b>	c1	c2	<b>VEE Core</b>
<b>GND</b>	c3	c4	<b>VFF RAM</b>
<b>USB-D0</b>	c5	c6	
<b>USB-D1</b>	c7	c8	
<b>USB-D2</b>	c9	c10	
<b>USB-D3</b>	c11	c12	
<b>USB-D4</b>	c13	c14	
<b>USB-D5</b>	c15	c16	
<b>USB-D6</b>	c17	c18	
<b>USB-D7</b>	c19	c20	
<b>USB-NXT</b>	c21	c22	
<b>USB-DIR</b>	c23	c24	
<b>USB-STP</b>	c25	c26	
<b>USB-PWFLT</b>	c27	c28	
	c29	c30	
	c31	c32	
<b>USB-CLK</b>	c33	c34	
<b>GND</b>	c35	c36	<b>GND</b>
<b>GND</b>	c37	c38	<b>GND</b>
<b>STDBY</b>	c39	c40	<b>LCSE</b>
<b>VDD</b>	c41	c42	<b>VDD</b>
<b>VDD</b>	c43	c44	<b>VDD</b>
<b>VDD</b>	c45	c46	<b>VDD</b>
<b>VDD</b>	c47	c48	<b>VDD</b>
<b>VDD</b>	c49	c50	<b>VDD</b>
<b>VDD</b>	c52	c51	<b>VDD</b>

<b>GND</b>	d1	d2	<b>SDC-CLK</b>
<b>GND</b>	d3	d4	<b>SDC-CMD</b>
	d5	d6	<b>SDC-D0</b>
	d7	d8	<b>SDC-D1</b>
	d9	d10	<b>SDC-D2</b>
	d11	d12	<b>SDC-D3</b>
	d13	d14	<b>SPI-SEL0</b>
	d15	d16	<b>SPI-SEL1</b>
<b>SPI-MOSI</b>	d17	d18	<b>SPI-SEL2</b>
<b>SPI-MISO</b>	d19	d20	<b>SPI-SEL3</b>
	d21	d22	<b>GND</b>
<b>SPI-CLK</b>	d23	d24	<b>GND</b>
	d25	d26	
	d27	d28	
	d29	d30	
	d31	d32	
<b>I2C1-SDA</b>	d33	d34	<b>UTXD1</b>
<b>I2C1-SCL</b>	d35	d36	<b>URXD1</b>
<b>I2C2-SDA</b>	d37	d38	<b>URTS1#</b>
<b>I2C2-SCL</b>	d39	d40	<b>UCTS1#</b>
<b>TMPD+</b>	d41	d42	
<b>TMPD-</b>	d43	d44	<b>UTXD2</b>
	d45	d46	<b>URXD2</b>
	d47	d48	<b>URTS2#</b>
<b>GND</b>	d49	d50	<b>UCTS2#</b>
<b>GND</b>	d51	d52	

## 16. DDR-II SDRAM Memory

The DDR SDRAM memory of the P2020 consists of nine 8bit wide singel or dual die devices and offer an 8 bit wide ECC. It is accessed via the MCS0# and MCS1# select lines of the P2020 processor and the used DRAM types have an organization of xx row and xx column addresses. The eight chip internal banks are accessed via the MBA0, MBA1 and MBA2 signals.

### 16.1. Memory Bus Pin Configuration

<b>P2020 Signal</b>	<b>DDR-SDRAM Function</b>
MDQ(63:0)	Data Bus
MEC(7:0)	ECC Data Bus
MDM(8:0)	Data Mask
MDQS(8:0)/ MDQS(8:0)#	Data Strobe
MBA(2:0)	Bank Select
MA(15:0)	Address-Bus
MCAS#	Column Address
MRAS#	Row Address
MWE#	Write Enable
MCS(0:1)#	Chip Select Lines
MCS(2:3)#	not used
MVREF	Reference Voltage
MCKE(0:1)	Clock Enable
MCKE(1:3)	not used
MCLK(1:5) / MCLK(1:5)#	DRAM Clock
MCLK0 / MCLK0#	not used
MODT(0:1)	on-die termination
MODT(2:3)	not used
MAPAR-ERR	not used, tied to high
MAPAR-OUT	not used

## 16.2. DDR SDRAM CS0-BNDS Register

Addr. 0xE0002000 Value 0x0000003F

MSB	Name	Description	Value	Selection	HEX
Bit 0	---	reserved	0		0
Bit 1	---		0		
Bit 2	---		0		
Bit 3	---		0		
Bit 4	SA	Starting Address	0	Address bit MSB	0
Bit 5	SA		0		
Bit 6	SA		0		
Bit 7	SA		0		
Bit 8	SA	Starting Address	0		0
Bit 9	SA		0		
Bit 10	SA		0		
Bit 11	SA		0		
Bit 12	SA	Starting Address	0		0
Bit 13	SA		0		
Bit 14	SA		0		
Bit 15	SA		0	Address bit LSB	
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	EA	Ending Address	0	Address bit MSB	0
Bit 21	EA		0		
Bit 22	EA		0		
Bit 23	EA		1		
Bit 24	EA	Ending Address	0		3
Bit 25	EA		0		
Bit 26	EA		1		
Bit 27	EA		1		
Bit 28	EA	Ending Address	1	xxMByte	F
Bit 29	EA		1		
Bit 30	EA		1		
Bit 31	EA		1	Address bit LSB	
<b>LSB</b>	<b>name</b>	<b>description</b>	<b>value</b>	<b>selection</b>	<b>HEX</b>

### 16.3. DDR SDRAM CS0-CONFIG Register

Addr. 0xE0002080 Value 0x80014202

MSB	Name	Description	Value	Selection	HEX	
Bit 0	CS0-EN	chip select enable	1	active	8	
Bit 1	---	reserved	0			
Bit 2	---		0			
Bit 3	---		0			
Bit 4	---	reserved	0		0	
Bit 5	---		0			
Bit 6	---		0			
Bit 7	---		0			
Bit 8	AP-EN	auto precharge enable	0	not active	0	
Bit 9	ODT-RD-CFG	read on-die termination	0			
Bit 10	ODT-RD-CFG		0	never		
Bit 11	ODT-RD-CFG		0			
Bit 12	---	reserved	0		1	
Bit 13	ODT-WR-CFG	write on-die termination	0			
Bit 14	ODT-WR-CFG		0	on CS active		
Bit 15	ODT-WR-CFG		1			
Bit 16	BA-BITS	number of bank bits	0	3 BITS	4	
Bit 17	BA-BITS		1			
Bit 18	---		0			
Bit 19	---		0			
Bit 20	---	reserved	0		2	
Bit 21	ROW-BITS	number of row address lines	0	14 row addresses		
Bit 22	ROW-BITS		1			
Bit 23	ROW-BITS		0			
Bit 24	---	reserved	0		0	
Bit 25	---		0			
Bit 26	---		0			
Bit 27	---		0			
Bit 28	---	reserved	0		2	
Bit 29	COL-BITS	number of column address lines	0	10 column addresses		
Bit 30	COL-BITS		1			
Bit 31	COL-BITS		0			
<b>LSB</b>	<b>name</b>	<b>description</b>	<b>value</b>	<b>selection</b>	<b>HEX</b>	

## 16.4. DDR-SDRAM-CS0-CFG2 Register

Addr. 0xE00020C0 Value 0x00000000

MSB	Name	Description	Value	Selection	HEX
Bit 0	---	RESERVED	1		0
Bit 1	---		1		
Bit 2	---		1		
Bit 3	---		0		
Bit 4	---	reserved	0	disabled	0
Bit 5	PASR-CFG	partial array self refresh	0		
Bit 6	PASR-CFG		1		
Bit 7	PASR-CFG		1		
Bit 8	---	RESERVED	0		0
Bit 9	---		0		
Bit 10	---		0		
Bit 11	---		0		
Bit 12	---	reserved	0		0
Bit 13	---		0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	---	reserved	0		0
Bit 21	---		0		
Bit 22	---		0		
Bit 23	---		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	---	reserved	0		0
Bit 29	---		0		
Bit 30	---		0		
Bit 31	---		0		
LSB	Name	Description	Value	Selection	HEX

## 16.5. DDR SDRAM CS1-BNDS Register

Addr. 0xE0002008 Value 0x0040007F

MSB	Name	Description	Value	Selection	HEX
Bit 0	---	reserved	0		0
Bit 1	---		0		
Bit 2	---		0		
Bit 3	---		0		
Bit 4	SA	Starting Address	0	Address bit MSB	0
Bit 5	SA		0		
Bit 6	SA		0		
Bit 7	SA		0		
Bit 8	SA	Starting Address	0		4
Bit 9	SA		1		
Bit 10	SA		0		
Bit 11	SA		0		
Bit 12	SA	Starting Address	0		0
Bit 13	SA		0		
Bit 14	SA		0		
Bit 15	SA		0	Address bit LSB	
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	EA	Ending Address	0	Address bit MSB	0
Bit 21	EA		0		
Bit 22	EA		0		
Bit 23	EA		1		
Bit 24	EA	Ending Address	0		7
Bit 25	EA		1		
Bit 26	EA		1		
Bit 27	EA		1		
Bit 28	EA	Ending Address	1	xxMByte	F
Bit 29	EA		1		
Bit 30	EA		1		
Bit 31	EA		1	Address bit LSB	
<b>LSB</b>	<b>name</b>	<b>description</b>	<b>value</b>	<b>selection</b>	<b>HEX</b>

## 16.6. DDR SDRAM CS1-CONFIG Register

Addr. 0xE0002088 Value 0x80014202

MSB	Name	Description	Value	Selection	HEX	
Bit 0	CS1-EN	chip select enable	1	active	8	
Bit 1	---	reserved	0			
Bit 2	---		0			
Bit 3	---		0			
Bit 4	---	reserved	0		0	
Bit 5	---		0			
Bit 6	---		0			
Bit 7	---		0			
Bit 8	AP-EN	auto precharge enable	0	not active	0	
Bit 9	ODT-RD-CFG	read on-die termination	0			
Bit 10	ODT-RD-CFG		0	never		
Bit 11	ODT-RD-CFG		0			
Bit 12	---	reserved	0		1	
Bit 13	ODT-WR-CFG	write on-die termination	0			
Bit 14	ODT-WR-CFG		0	on CS active		
Bit 15	ODT-WR-CFG		1			
Bit 16	BA-BITS	number of bank bits	0	3 BITS	4	
Bit 17	BA-BITS		1			
Bit 18	---		0			
Bit 19	---		0			
Bit 20	---	reserved	0		2	
Bit 21	ROW-BITS	number of row address lines	0	14 row addresses		
Bit 22	ROW-BITS		1			
Bit 23	ROW-BITS		0			
Bit 24	---	reserved	0		0	
Bit 25	---		0			
Bit 26	---		0			
Bit 27	---		0			
Bit 28	---	reserved	0		2	
Bit 29	COL-BITS	number of column address lines	0	10 column addresses		
Bit 30	COL-BITS		1			
Bit 31	COL-BITS		0			
<b>LSB</b>	<b>name</b>	<b>description</b>	<b>value</b>	<b>selection</b>	<b>HEX</b>	

## 16.7. DDR-SDRAM-CS1-CFG2 Register

Addr. 0xE00020C8 Value 0x00000000

MSB	Name	Description	Value	Selection	HEX
Bit 0	---	RESERVED	1		0
Bit 1	---		1		
Bit 2	---		1		
Bit 3	---		0		
Bit 4	---	reserved	0	disabled	0
Bit 5	PASR-CFG	partial array self refresh	0		
Bit 6	PASR-CFG		1		
Bit 7	PASR-CFG		1		
Bit 8	---	RESERVED	0		0
Bit 9	---		0		
Bit 10	---		0		
Bit 11	---		0		
Bit 12	---	reserved	0		0
Bit 13	---		0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	---	reserved	0		0
Bit 21	---		0		
Bit 22	---		0		
Bit 23	---		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	---	reserved	0		0
Bit 29	---		0		
Bit 30	---		0		
Bit 31	---		0		
LSB	Name	Description	Value	Selection	HEX

## 16.8. DDR-SDRAM-CFG1 Register

Addr. 0xE0002110 Value 0xE3000000

MSB	Name	Description	Value	Selection	HEX
Bit 0	MEM-EN	SDRAM interface enable	1	SDRAM active	E
Bit 1	SR-EN	Self refresh enable	1	enabled	
Bit 2	ECC-EN	ECC enable	1	ECC active	
Bit 3	RD-EN	Registered DIMM enable	0	unbuffered	
Bit 4	---	reserved	0		3
Bit 5	SDR-TYPE	SDRAM TYPE	0	DDR-II-SDRAM	
Bit 6	SDR-TYPE		1		
Bit 7	SDR-TYPE		1		
Bit 8	---	reserved	0		0
Bit 9	---		0		
Bit 10	DYN-PWR	Dynamic power management	0	disabled	0
Bit 11	DBW	DRAM data bus width	0	64 bit	
Bit 12	DBW		0	64 bit	
Bit 13	8-BE	8 beat burst enable	0	4 beat burst	0
Bit 14	NCAP	Non-concurrent auto precharge	0	concurrent modus	
Bit 15	3T-EN	3T timing enable	0		
Bit 16	2T-EN	2T timing enable	0	1T-Modus	0
Bit 17	BA-INTLV	bank interleave control	0	no interleave	
Bit 18	BA-INTLV		0		
Bit 19	BA-INTLV		0		
Bit 20	BA-INTLV	bank interleave control	0	no interleave	0
Bit 21	BA-INTLV		0		
Bit 22	BA-INTLV		0		
Bit 23	BA-INTLV		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	X32-EN	DRAM organization	0	x8 devices	0
Bit 27	PCHB8	precharge bit 8 enable	0	MA10	
Bit 28	HSE	half strength drive enable	0	disabled	0
Bit 29	---	reserved	0		
Bit 30	MEM-HLT	DDR memory controller halt	0	normal operation	
Bit 31	BI	bypass initialization	0	hardware init	
LSB	Name	Description	Value	Selection	HEX

## 16.9. DDR-SDRAM-CFG2 Register

Addr. 0xE0002114 Value 0x04401010

MSB	Name	Description	Value	Selection	HEX
Bit 0	FRC-SR	force self refresh	0	normal operation	0
Bit 1	SR-IE	self refresh interrupt enable	0	no self refresh mode	
Bit 2	DLL-RST	DLL reset disable	0	DLL reset enabled	
Bit 3	---	reserved	0		
Bit 4	DQS-CFG	DQS configuration	0	differential mode	4
Bit 5	DQS-CFG		1		
Bit 6	---	reserved	0		
Bit 7	---		0		
Bit 8	---	reserved	0		4
Bit 9	ODT-CFG	OnDieTermination Configuration	1	on read only	
Bit 10	ODT-CFG		0		
Bit 11	---	reserved	0		
Bit 12	---	reserved	0		0
Bit 13	---		0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	NUM-PR	number of posted refreshes	0	1	1
Bit 17	NUM-PR		0		
Bit 18	NUM-PR		0		
Bit 19	NUM-PR		1		
Bit 20	---	reserved	0		0
Bit 21	---		0		
Bit 22	---		0		
Bit 23	---		0		
Bit 24	---	RESERVED	0		1
Bit 25	OBC-CFG	on the fly burst chop	0	off	
Bit 26	AP-EN	address parity enable	0	off	
Bit 27	D-INIT	dram initialization	0	on	
Bit 28	---	RESERVED	0		0
Bit 29	RCW-EN	DDR3 register ctl. enable	0	off	
Bit 30	---	reserved	0		
Bit 31	MD-EN	mirrored DIMM enable	0	off	
LSB	Name	Description	Value	Selection	HEX

## 16.10. DDR-SDRAM-MODE-2 Register

Addr. 0xE000211C Value 0x00000000

MSB	name	description	value	selection	HEX
Bit 0		Extended SDRAM-Mode 2	0		0
Bit 1			0		
Bit 2			0		
Bit 3			0		
Bit 4		Extended SDRAM-Mode 2	0		0
Bit 5			0		
Bit 6			0		
Bit 7			0		
Bit 8	SRT	Extended SDRAM-Mode 2	0	1x refresh rate	0
Bit 9			0		
Bit 10			0		
Bit 11			0		
Bit 12		Extended SDRAM-Mode2	0		0
Bit 13			0		
Bit 14			0		
Bit 15			0		
Bit 16		Extended SDRAM-Mode 3	0		0
Bit 17			0		
Bit 18			0		
Bit 19			0		
Bit 20		Extended SDRAM-Mode 3	0		0
Bit 21			0		
Bit 22			0		
Bit 23			0		
Bit 24		Extended SDRAM-Mode 3	0		0
Bit 25			0		
Bit 26			0		
Bit 27			0		
Bit 28		Extended SDRAM-Mode3	0		0
Bit 29			0		
Bit 30			0		
Bit 31			0		
LSB	name	description	value	selection	HEX

## 16.11. DDR-SDRAM-MD-CNTL Register

Addr. 0xE0002120 Value 0x0000000

MSB	name	description	value	selection	HEX
Bit 0	MD-EN	mode enable	0		0
Bit 1	---	reserved	0		
Bit 2	CS-SEL	active cs line	0	CS0 is active	0
Bit 3	CS-SEL		0		
Bit 4	---		0		
Bit 5	MD-SEL	mode register select	0	0	
Bit 6	MD-SEL		0		
Bit 7	MD-SEL		0		
Bit 8	SET-REF	set refresh	0		0
Bit 9	SET-PRE	set precharge	0		
Bit 10	CKE-CNTL	clock enable control	0		0
Bit 11	CKE-CNTL		0		
Bit 12	---		0		
Bit 13	---		0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	MD-VALUE	mode register value	0	0	0
Bit 17	MD-VALUE		0		
Bit 18	MD-VALUE		0		
Bit 19	MD-VALUE		0		
Bit 20	MD-VALUE	mode register value	0	0	0
Bit 21	MD-VALUE		0		
Bit 22	MD-VALUE		0		
Bit 23	MD-VALUE		0		
Bit 24	MD-VALUE	mode register value	0	0	0
Bit 25	MD-VALUE		0		
Bit 26	MD-VALUE		0		
Bit 27	MD-VALUE		0		
Bit 28	MD-VALUE	mode register value	0	0	0
Bit 29	MD-VALUE		0		
Bit 30	MD-VALUE		0		
Bit 31	MD-VALUE		0		
LSB	name	description	value	selection	HEX

## 16.12. DDR SDRAM Timing-CFG-0 Register

Addr: 0x00002104 Value 0x00280802

MSB	Name	Description	Value	Selection	HEX
Bit 0	RWT	read to write turnaround	0	5 Clock Cycles	0
Bit 1	RWT		0		
Bit 2	WRT	write to read turnaround	0	4 Clock Cycles	
Bit 3	WRT		0		
Bit 4	RRT	read to read turnaround	0	3 Clock Cycles	0
Bit 5	RRT		0		
Bit 6	WWT	write to write turnaround	0	2 Clock Cycles	
Bit 7	WWT		0		
Bit 8	---	reserved	0		2
Bit 9	ACT-PD-EXT	t(xard)	0	2 Clock Cycles	
Bit 10	ACT-PD-EXT		1		
Bit 11	ACT-PD-EXT		0		
Bit 12	PRE-PD-EXT	t(xp)	1	8 Clock Cycles	8
Bit 13	PRE-PD-EXT		0		
Bit 14	PRE-PD-EXT		0		
Bit 15	PRE-PD-EXT		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	---		0		
Bit 20	ODT-PD-EXT	t(axpd)	1	8 Clock Cycles	8
Bit 21	ODT-PD-EXT		0		
Bit 22	ODT-PD-EXT		0		
Bit 23	ODT-PD-EXT		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	MRS-CYC	t(mrd)	0	2 Clock Cycle	2
Bit 29	MRS-CYC		0		
Bit 30	MRS-CYC		1		
Bit 31	MRS-CYC		0		
<b>LSB</b>	<b>name</b>	<b>description</b>	<b>value</b>	<b>selection</b>	<b>HEX</b>

### 16.13. DDR SDRAM Timing-CFG-1 Register

Addr. 0xE0002108 Value 0x5E593533

MSB	Name	Description	Value	Selection	HEX
Bit 0	PRETOACT	t(rp)	0	5 clock cycles	5
Bit 1	PRETOACT		1		
Bit 2	PRETOACT		0		
Bit 3	PRETOACT		1		
Bit 4	ACTTOPRE	t(ras)	1	14 clock cycles	E
Bit 5	ACTTOPRE		1		
Bit 6	ACTTOPRE		1		
Bit 7	ACTTOPRE		0		
Bit 8	ACTTORW	t(rcd)	0	5 clock cycles	5
Bit 9	ACTTORW		1		
Bit 10	ACTTORW		0		
Bit 11	ACTTORW		1		
Bit 12	CASLAT	t(cl)	1	9 clock cycles	9
Bit 13	CASLAT		0		
Bit 14	CASLAT		0		
Bit 15	CASLAT		1		
Bit 16	REFREC	t(rfc)	0	8+32+3 clock cycles	3
Bit 17	REFREC		0		
Bit 18	REFREC		1		
Bit 19	REFREC		1		
Bit 20	WRREC	t(wr)	0	5 clock cycles	5
Bit 21	WRREC		1		
Bit 22	WRREC		0		
Bit 23	WRREC		1		
Bit 24	---	reserved	0		3
Bit 25	ACTTOACT	t(rrd)	0	3 clock cycles	
Bit 26	ACTTOACT		1		
Bit 27	ACTTOACT		1		
Bit 28	---	reserved	0		3
Bit 29	WRTORD	t(wtr)	0	3 clock cycles	
Bit 30	WRTORD		1		
Bit 31	WRTORD		1		
LSB	name	description	value	selection	HEX

## 16.14. DDR SDRAM Timing-CFG-2 Register

Addr. 0xE000210C Value 0x0FA06CCD

MSB	name	description	value	selection	HEX
Bit 0	ADD-LAT	t(al)	0	0 clock cycles	0
Bit 1	ADD-LAT		0		
Bit 2	ADD-LAT		0		
Bit 3	ADD-LAT		0		
Bit 4	CPO	MCAS-to-preamble override	1	autodetect	F
Bit 5	CPO		1		
Bit 6	CPO		1		
Bit 7	CPO		1		
Bit 8	CPO		1		A
Bit 9	WR-LAT	t(wl)	0	4 clock cycles	
Bit 10	WR-LAT		1		
Bit 11	WR-LAT		0		
Bit 12	WR-LAT	T(WL)	0	4 clock cycles	0
Bit 13	---	RESERVED	0		
Bit 14	---		0		
Bit 15	---		0		
Bit 16	RD-TO-PRE	t(rtp)	0	3 clock cycles	6
Bit 17	RD-TO-PRE		1		
Bit 18	RD-TO-PRE		1		
Bit 19	WRD-DLY	write data delay	0	3 clock cycles	
Bit 20	WRD-DLY	write data delay	1	3 clock cycles	C
Bit 21	WRD-DLY		1		
Bit 22	---		0		
Bit 23	CKE-PLS	T(CKE)	0		
Bit 24	CKE-PLS	t(cke)	1	3 clock cycles	C
Bit 25	CKE-PLS		1		
Bit 26	FOUR-ACT	t(faw)	0	9 clock cycles	
Bit 27	FOUR-ACT		0		
Bit 28	FOUR-ACT	t(faw)	1	13 clock cycles	D
Bit 29	FOUR-ACT		1		
Bit 30	FOUR-ACT		0		
Bit 31	FOUR-ACT		1		
LSB	name	description	value	selection	HEX

### 16.15. DDR SDRAM Timing-CFG-3 Register

Addr. 0xE0002100 Value 0x00020000

MSB	name	description	value	selection	HEX
Bit 0	---	reserved	0		0
Bit 1	---		0		
Bit 2	---		0		
Bit 3	---		0		
Bit 4	---	reserved	0		0
Bit 5	---		0		
Bit 6	---		0		
Bit 7	EXT- ACTTOPRE	extended t(ras)	0		
Bit 8	---	reserved	0		0
Bit 9	---		0		
Bit 10	---		0		
Bit 11	---		0		
Bit 12	EXT-REFREC	t(rfc)	0	2 X 16 CLOCKS	2
Bit 13	EXT-REFREC		0		
Bit 14	EXT-REFREC		0		
Bit 15	EXT-REFREC		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	---		0		
Bit 19	EXT-CASLAT		0		
Bit 20	---	reserved	0		0
Bit 21	---		0		
Bit 22	---		0		
Bit 23	---		0		
Bit 24	---	reserved	0		0
Bit 25	---		0		
Bit 26	---		0		
Bit 27	---		0		
Bit 28	---	reserved	0	CLOCK ALIGNED	0
Bit 29	CNTL-ADJ	CONTROL ADJUST	0		
Bit 30	CNTL-ADJ		0		
Bit 31	CNTL-ADJ		0		
LSB	name	description	value	selection	HEX

## 16.16. DDR-SDRAM-INTERVAL Register

Addr. 0xE0002124 Value 0x05120100

MSB	Name	Description	Value	Selection	HEX
Bit 0	REFINT	refresh interval	0		0
Bit 1	REFINT		0		
Bit 2	REFINT		0		
Bit 3	REFINT		0		
Bit 4	REFINT	refresh interval	0		5
Bit 5	REFINT		1		
Bit 6	REFINT		0		
Bit 7	REFINT		1		
Bit 8	REFINT	refresh interval	0	3.9us @ 333MHZ DDR Clock	1
Bit 9	REFINT		0		
Bit 10	REFINT		0		
Bit 11	REFINT		1		
Bit 12	REFINT	refresh interval	0		2
Bit 13	REFINT		0		
Bit 14	REFINT		1		
Bit 15	REFINT		0		
Bit 16	---	reserved	0		0
Bit 17	---		0		
Bit 18	BSTOPRE	precharge interval	0		
Bit 19	BSTOPRE		0		
Bit 20	BSTOPRE	precharge interval	0		1
Bit 21	BSTOPRE		0		
Bit 22	BSTOPRE		0		
Bit 23	BSTOPRE		1		
Bit 24	BSTOPRE	precharge interval	0	256 clocks	0
Bit 25	BSTOPRE		0		
Bit 26	BSTOPRE		0		
Bit 27	BSTOPRE		0		
Bit 28	BSTOPRE	precharge interval	0		0
Bit 29	BSTOPRE		0		
Bit 30	BSTOPRE		0		
Bit 31	BSTOPRE		0		
LSB	name	description	value	selection	HEX

## 16.17. DDR-SDRAM-MODE Register

Addr 0x00002118 Value 0x00040852

MSB	name	description	value	selection	HEX
Bit 0	MRS/EMRS	Extended SDRAM-Mode	0	set to EMRS	0
Bit 1	MRS/EMRS		0		
Bit 2	0		0		
Bit 3	Outputs		0	enabled	
Bit 4	RDQS enable	Extended SDRAM-Mode	0	no	0
Bit 5	DQS enable		0	enabled	
Bit 6	OCD operation		0		
Bit 7	OCD operation		0	no OCD operation	
Bit 8	OCD operation	Extended SDRAM-Mode	0		0
Bit 9	RTT		1	75R	
Bit 10	posted CAS		0		
Bit 11	posted CAS		0	AL = 0	
Bit 12	posted CAS	Extended SDRAM-Mode	0		4
Bit 13	RTT		0	75R	
Bit 14	drive strength		0	full strength driver	
Bit 15	DLL enable		0	DLL enabled	
Bit 16	MRS/EMRS	SDRAM-Mode	0		0
Bit 17	MRS/EMRS		0	set to MRS	
Bit 18	0		0		
Bit 19	pd mode		0	fast exit	
Bit 20	write recovery	SDRAM-Mode	1	T(WR) = 5	8
Bit 21	write recovery		0		
Bit 22	write recovery		0		
Bit 23	DLL reset		0	no	
Bit 24	TM mode	SDRAM-Mode	0	normal	5
Bit 25	CAS latency		1	CAS Latency = 5	
Bit 26	CAS latency		0		
Bit 27	CAS latency		1		
Bit 28	burst type	SDRAM-Mode	0	Sequential	2
Bit 29	burst length		0	Burst Length 4	
Bit 30	burst length		1		
Bit 31	burst length		0		
LSB	name	description	value	selection	HEX

## 17. NAND Flash Memory

The flash memory of the P2020 consists of a single NAND device with a 8-bit wide data bus. The used 2Gbit device is controlled via select line LCS0# and the FCM controller of the P2020.

It is used as boot ROM after power on. The boot ROM location is defined by the four POR configuration signals MII1-TXD[6:4] and MII1-TXER. The state of these signals is controlled via the power up configuration PLD J21.

MII1-TXD6	MII1-TXD5	MII1-TXD4	MII1-TXER	boot ROM location
1	0	1	0	Local bus FCM 8-bit NAND flash large page

If any other LBC boot device should be connected to LCS0#, the local NAND flash can be disabled by setting the LCSE# line on connector ST2-c40 to high. The LCSE# signal is tied to GND by an onboard 1k0 resistor.

The flash device is write protected by default via the FLWP# signal on connector ST2-b38. If this signal is tied to BVDD, the NAND flash write protection is disabled. The FLWP# signal is tied to GND by an onboard 2k2 resistor.

The mounted NAND device works with 3.3V supply voltage, i.e. the BVSL0/1 setting must be configured for 3.3V I/O voltage. If any other I/O configuration is set for the LBC interface, the LCE# signal must be tied to 3.3V volts, to disable the onboard NAND device.

### 17.1. NAND Flash Pin Configuration

<b>P2020 LBC Signal</b>	<b>NAND Function</b>
LAD(7:0)	Address/Data Bus
LCS0#/LCSE#	Chip Select
LGPL2	Read Enable
LWE0#	Write Enable
LGPL1	Address Latch Enable
LGPL0	Command Latch Enable
LGPL4	Ready/Busy
LGPL3/FLWP#	Write Protect

## 17.2. BR0 Base Register

Addr. 0xE0005000 Value 0xFE00C21

MSB	Name	Description	Value	Selection	HEX
Bit 0	BA	base address	1	base address bit MSB	F
Bit 1	BA		1		
Bit 2	BA		1		
Bit 3	BA		1		
Bit 4	BA	base address	1		E
Bit 5	BA		1		
Bit 6	BA		1		
Bit 7	BA		0		
Bit 8	BA	base address	0		0
Bit 9	BA		0		
Bit 10	BA		0		
Bit 11	BA		0		
Bit 12	BA	base address	0		0
Bit 13	BA		0		
Bit 14	BA		0		
Bit 15	BA		0		
Bit 16	BA	base address	0	base address bit LSB	0
Bit 17	---	reserved	0		
Bit 18	---		0		
Bit 19	PS	port size	0	8 Bit	
Bit 20	PS	port size	1	8 Bit	C
Bit 21	DECC	data error correction	1	ecc check	
Bit 22	DECC		0		
Bit 23	WP	write protect	0	not write protected	
Bit 24	MSEL	machine select	0	FCM	2
Bit 25	MSEL		0		
Bit 26	MSEL		1		
Bit 27	---	reserved	0		
Bit 28	ATOM	atomic operation	0	no atomic operations	1
Bit 29	ATOM		0		
Bit 30	---	reserved	0		
Bit 31	V	valid bit	1	1 = CS active	
LSB	name	description	value	selection	HEX

### 17.3. OR0 Option Register

Addr. 0xE0005004 Value 0xF0000C72

MSB	name	description	value	selection	HEX
Bit 0	AM	address mask	1	address mask MSB	F
Bit 1	AM		1		
Bit 2	AM		1		
Bit 3	AM		1		
Bit 4	AM	address mask	0		0
Bit 5	AM		0		
Bit 6	AM		0		
Bit 7	AM		0		
Bit 8	AM	address mask	0		0
Bit 9	AM		0		
Bit 10	AM		0		
Bit 11	AM		0		
Bit 12	AM	address mask	0		0
Bit 13	AM		0		
Bit 14	AM		0		
Bit 15	AM		0		
Bit 16	AM	address mask	0	address mask LSB	0
Bit 17	---	reserved	0		
Bit 18	---		0		
Bit 19	BCTLD	Data Buffer Control Disable	0	LBCTL active	
Bit 20	---	reserved	0		7
Bit 21	PGS	NAND page size	1	2048+64 bytes	
Bit 22	CSCT	LCS# to command time	1	8 clocks	
Bit 23	CST	command setup time	1	1 clock	
Bit 24	CHT	command hold time	1	2 clocks	A
Bit 25	SCY	wait states & cycle length	0		
Bit 26	SCY		1		
Bit 27	SCY		0		
Bit 28	RST	read setup time	1	1 clock	E
Bit 29	TRLX	CSCT/CST/CHT/RST MSB	1	set	
Bit 30	EHTR	extended Hold time on Read	1	+ 8 idle clocks	
Bit 31	---	reserved	0		
LSB	name	description	value	selection	HEX

## 18. I<sup>2</sup>C Temperature Sensor

### 18.1. Temperature Sensor I<sup>2</sup>C Access Address

<i>Device</i>	<i>Hex</i>	<i>7 bit binary I<sup>2</sup>C address</i>							<i>read/write</i>
DS75LV	0x4F	1	0	0	1	1	1	1	1/0

The MPX2020 contains a temperature sensor near the cpu on top of the pcb, which allows for a thermal connection to a mounted cooling device. The thermostat output of the device is not used. The DS75LV uses a single 8-bit address word following the shown device address.

## 19. I<sup>2</sup>C EEPROM-I

### 19.1. EEPROM-I I<sup>2</sup>C Access Address

<i>Device</i>	<i>Hex</i>	<i>7 bit binary I<sup>2</sup>C address</i>							<i>read/write</i>
AT24C128	0x50	1	0	1	0	0	0	0	1/0

The AT24C128 uses a two 8-bit address word following the shown device address for data access. The write protect function of the first Atmel EEPROM device is disabled.

## 20. I<sup>2</sup>C EEPROM-II

### 20.1. EEPROM-II I<sup>2</sup>C Access Address

<i>Device</i>	<i>Hex</i>	<i>7 bit binary I<sup>2</sup>C address</i>							<i>read/write</i>
AT24C128	0x52	1	0	1	0	0	1	0	1/0

The AT24C128 uses a two 8-bit address word following the shown device address for data access. The write protect function of the second Atmel EEPROM device controlled via the FLWP# pin on connector ST2.b38. This pin is tied to low via a 4K7 pulldown resistor.

## 21. I<sup>2</sup>C Real Time Clock

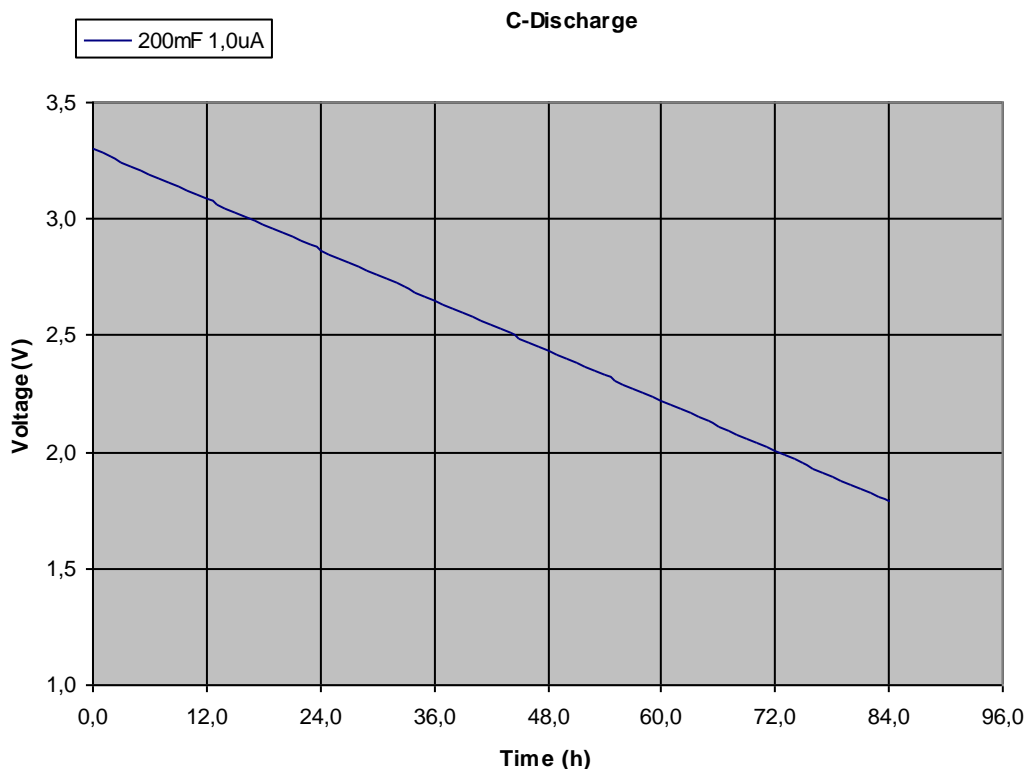
### 21.1. RTC I<sup>2</sup>C Access Addresses

Device	Hex	7 bit binary I <sup>2</sup> C address							read/write
ISL12020	0x57	1	0	1	0	1	1	1	1/0
ISL12020	0x6F	1	1	0	1	1	1	1	1/0

The the ISL12020 uses a single 8-bit address word following the shown device address for data access. It offers two access addresses, one for the register set, the second for the user SRAM. The interrupt line of the ISL12020 is connected to the processor line IRQ0# via the solder link RIRQ.

The backup function of the RTC is supported by an onboard gold capacitor for short time sequences. If the the backup time should be extended, an external supply must be connected to STDBY on connector ST2.c39

### 21.2. RTC Gold Cap Backup Time @25°C



## 21.3. RTC Address Map

Addr.	Section	Register	D7	D6	D5	D4	D3	D2	D1	D0	Range	default
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h	RTC	MN	0	MN22	MN21	MN20	MN13	MN12	MN	MN12	0 to 59	00h
02h	RTC	HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h	RTC	DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
04h	RTC	MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
05h	RTC	YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h	RTC	DW	0	0	0	0	0	DW2	DW1	DW0	0 to 6	00h
07h	CSR	SR	BUSY	OSCF	DSTADJ	ALM	LVDD	LBAT85	LBAT75	RTCF	N/A	01h
08h	CSR	INT	ARST	WRTC	IM	FOBATB	FO3	FO2	FO1	FO0	N/A	01h
09h	CSR	PWR_VDD	CLRTS	D	D	D	D	VDDTrip2	VDDTrip1	VDDTrip0	N/A	00h
0Ah	CSR	PWR_VBAT		RESEALB	VB85Tp2	VB85Tp1	VB85Tp0	VB75Tp2	VB75Tp1	VB75Tp0	N/A	00h
0Bh	CSR	ITRO	IDTR01	IDTR00	IATR05	IATR04	IATR03	IATR02	IATR01	IATR00	N/A	20h
0Ch	CSR	ALPHA	ALPHA7	ALPHA6	ALPHA5	ALPHA4	ALPHA3	ALPHA2	ALPHA1	ALPHA0	N/A	46h
0Dh	CSR	BETA	TSE	BTSE	BTSR	BETA4	BETA3	BETA2	BETA1	BETA0	N/A	00h
0Eh	CSR	FATR	0	0	FFATR5	FATR4	FATR3	FATR2	FATR1	FATR0	N/A	00h
0Fh	CSR	FDTR	0	0	0	FDTR4	FDTR3	FDTR2	FDTR1	FDTR0	N/A	00h
10h	ALARM	SCA0	ESCA0	SCA022	SCA021	SCA020	SCA013	SCA012	SCA011	SCA010	0 to 59	00h
11h	ALARM	MNA0	EMNA0	MNA022	MNA021	MNA020	MNA013	MNA012	MNA011	MNA010	0 to 59	00h
12h	ALARM	HRA0	EHA0	D	HRA021	HRA020	HRA013	HRA012	HRA011	HRA010	0 to 23	00h
13h	ALARM	DTA0	EDTA0	D	DTA021	DTA020	DTA013	DTA012	DTA011	DTA010	1 to 31	00h
14h	ALARM	MOA0	EMOA00	D	D	MOA020	MOA013	MOA012	MOA011	MOA010	1 to 12	00h
15h	ALARM	DWA0	EDWA0	D	D	D	D	DWA02	DWA01	DWA00	0 to 6	00h
16h	TSV2B	VSC	0	VSC22	VSC21	VSC20	VSC13	VSC12	VSC11	VSC10	0 to 59	00h
17h	TSV2B	VMN	0	VMN22	VMN21	VMN20	VMN13	VMN12	VMN11	VMN10	0 to 59	00h
18h	TSV2B	VHR	VMIL	0	VHR21	VHR20	VHR13	VHR12	VHR11	VHR10	0 to 23	00h
19h	TSV2B	VDT	0	0	VDT21	VDT20	VDT13	VDT12	VDT11	VDT10	1 to 31	00h
1Ah	TSV2B	VMO	0	0	0	VMO20	VMO13	VMO12	VMO11	VMO10	1 to 12	00h
1Bh	TSV2B	BSC	0	BSC22	BSC21	BSC20	BSC13	BSC12	BSC11	BSC10	0 to 59	00h
1Ch	TSV2B	BMN	0	BMN22	BMN21	BMN20	BMN13	BMN12	BMN11	BMN10	0 to 59	00h
1Dh	TSV2B	BHR	BMIL	0	BHR21	BHR20	BHR13	BHR12	BHR11	BHR10	0 to 23	00h
1Eh	TSV2B	BDT	0	0	BDT21	BDT20	BDT13	BDT12	BDT11	BDT10	1 to 31	00h
1Fh	TSV2B	BMO	0	0	0	BMO20	BMO13	BMO12	BMO11	BMO10	1 to 12	00h
20h	DSTCR	DstMoFd	DSTE	D	D	DstMoFd20	DstMoFd13	DstMoFd12	DstMoFd11	DstMoFd10	1 to 12	00h
21h	DSTCR	DstDwFd	D	DstDwFdE	DstWkFd12	DstWkFd11	DstWkFd10	DstDwFd12	DstDwFd11	DstDwFd10	0 to 6	00h
22h	DSTCR	DstDtFd	D	D	DstDtFd21	DstDtFd20	DstDtFd13	DstDtFd12	DstDtFd11	DstDtFd10	1 to 31	00h
23h	DSTCR	DstHrFd	D	D	DstHrFd21	DstHrFd20	DstHrFd13	DstHrFd12	DstHrFd11	DstHrFd10	0 to 23	00h
24h	DSTCR	DstMoRv	D	D	D	XDstMoRv2	0	DstMoRv13	DstMoR12v	DstMoRv11	1 to 12	00h
25h	DSTCR	DstDwRv		DstDwRvE	DstWkRv12	DstWkRv11	DstWkRv10	DstDwRv12	DstDwRv11	DstDwRv10	0 to 6	00h
26h	DSTCR	DstDtRv	D	D	DstDtRv21	DstDtRv20	DstDtRv13	DstDtRv12	DstDtRv11	DstDtRv10	1 to 31	00h
27h	DSTCR	DstHrRv	D	D	DstHrRv21	DstHrRv20	DstHrRv13	DstHrRv12	DstHrRv11	DstHrRv10	0 to 23	00h
28h	TEMP	TK0L	TK07	TK06	TK05	TK04	TK03	TK02	TK01	TK00	00 to FF	00h
29h	TEMP	TK0M	0	0	0	0	0	0	TK09	TK08	00 to 03	00h
2Ah	NPPM	NPPML	NPPM7	NPPM6	NPPM5	NPPM4	NPPM3	NPPM2	NPPM1	NPPM0	00 to FF	00h
2Bh	NPPM	NPPMH	0	0	0	0	0	NPPM10	NPPM9	NPPM8	00 to 07	00h
2Ch	XT0	XT0	D	D	D	XT4	XT3	XT2	XT1	XT0	00 to FF	00h
2Dh	ALPHA	ALPHA_H	ALP_H7	ALP_H6	ALP_H5	ALP_H4	ALP_H3	ALP_H2	ALP_H1	ALP_H0	00 to 7F	46h
2Eh	GPM	GPM1	GPM17	GPM16	GPM15	GPM14	GPM13	GPM12	GPM11	GPM10	00 to FF	00h
2Fh	GPM	GPM2	GPM27	GPM26	GPM25	GPM24	GPM23	GPM22	GPM21	GPM20	00 to FF	00h

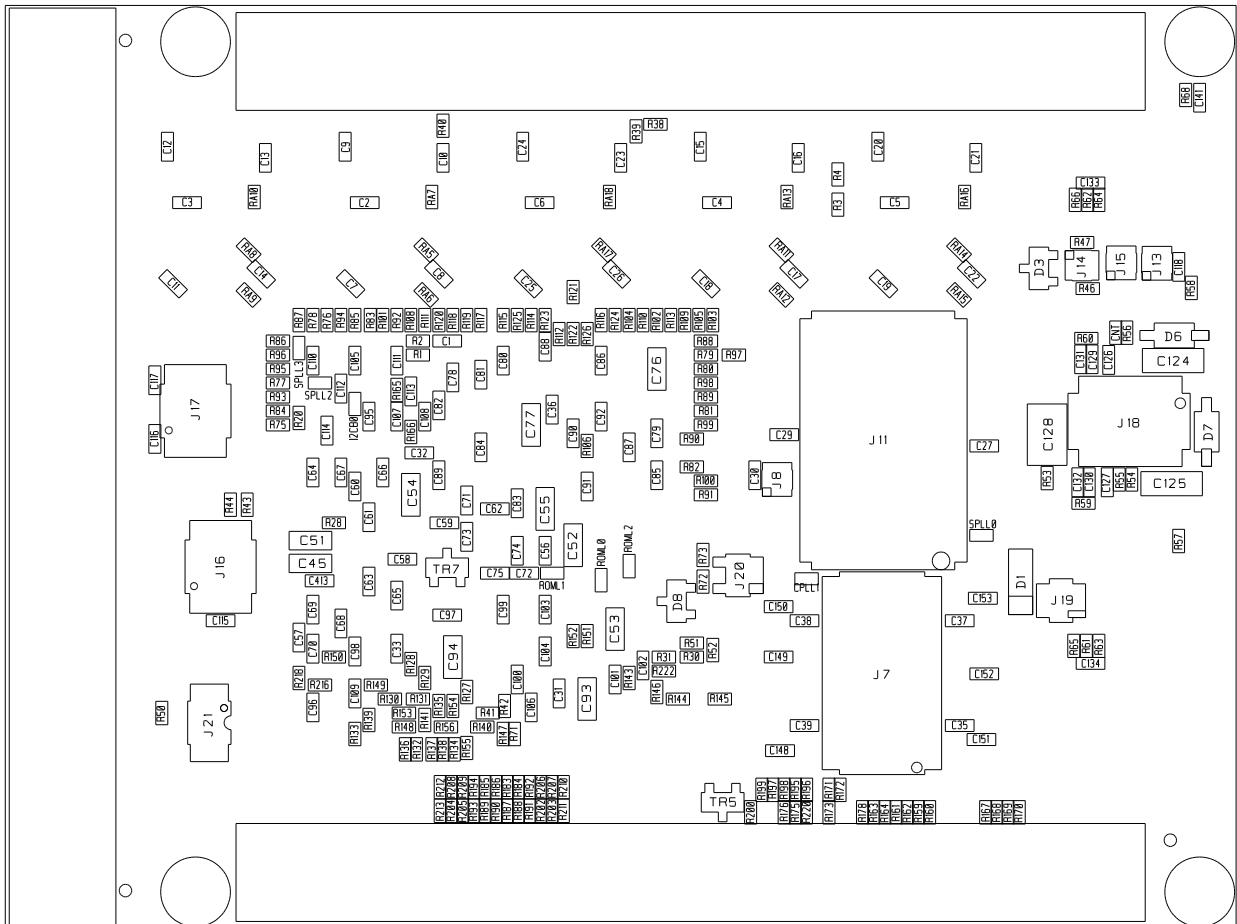
## 22. Hardware Watchdog Timer

The MPX2020 features a fixed rate hardware timer for watchdog purposes (MAX823), which can be enabled by software. Once enabled by a low active pulse (min. 50ns) to signal CSWDG#, it only can be disabled by a hardware reset. The time out rate is 1.6 seconds. Within that time at least one access must be performed to signal CSWDG#, to retrigger the timer. The signal CSWDG# leads to connector ST2.b44 and must be connected to a software controlable signal on the carrier board. Leaving this pin open disables the watchdog timer function at all.

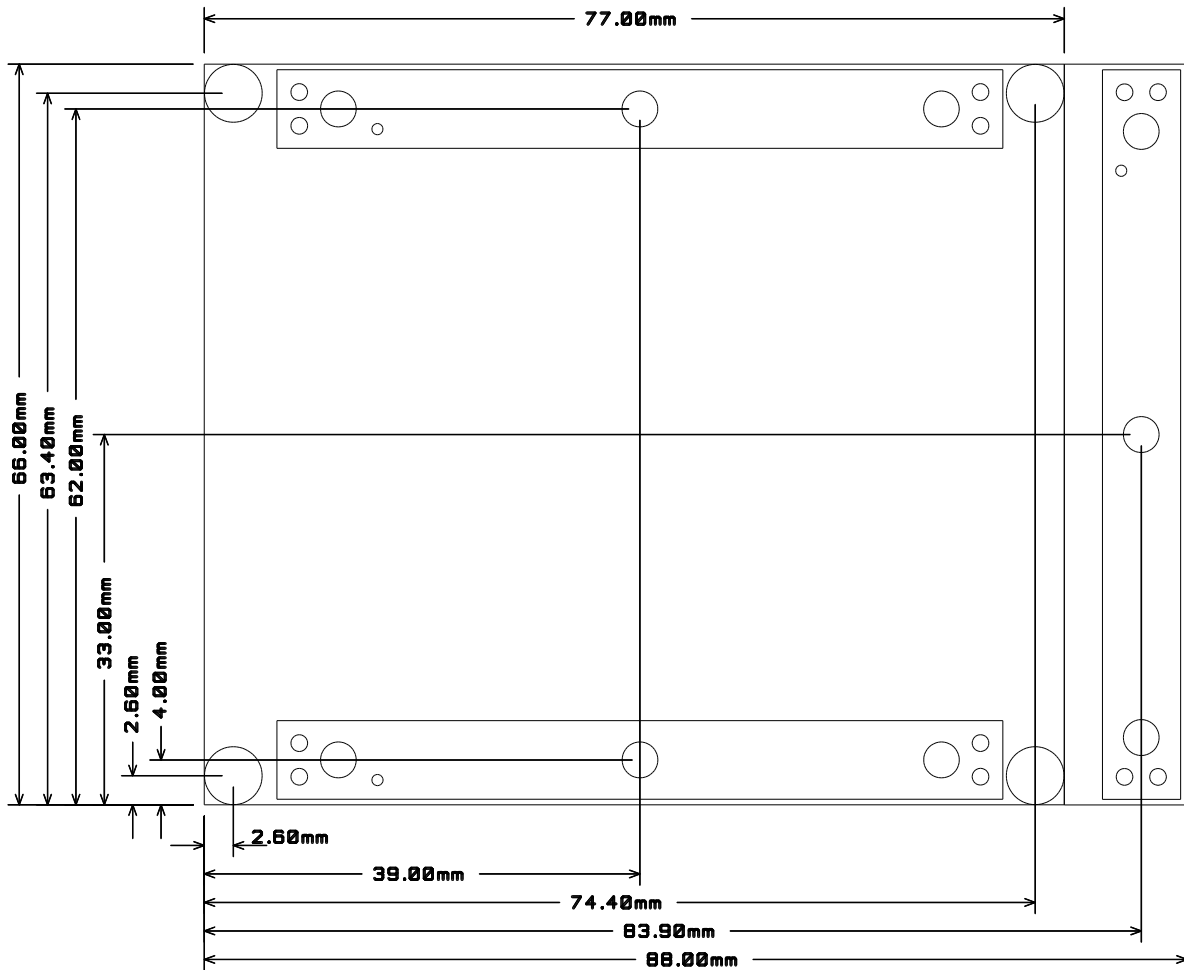
# Appendices



# Layout Solder Side



## Physical Dimensions (Top View)



## Schematics MPX2020 (please contact **MicroSys**)