Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
D-82054 Sauerlach
Germany

declare that the product

IPC 03

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date: 15.09.1998

Signature:

Position: General Manager

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User's Manual

IPC 03

2nd edition

Edition

	Date:	Ident-Nr.:	Released:
Manual	10.11.98	EW191MA-01AB	
Schematics	14.07.98	EW191SL-01AA	

Table of Contents

1. Introduction

1.1 Short Description

The **IPC03** is a double height board out of the MicroSys VMEbus line. It is used as a non intelligent carrier board for up to four 'IndustryPack'-compatible modules according to the Green Spring Logic Interface Specification Revision 0.7.1 for IP-Modules.

The **IPC03** supports all 8MHz, 8 or 16 bit, single or double IP-Modules with IO- and Memory-Cycles in non DMA mode. The interrupt structure is freely programmable not even for each slot, but also for both interrupt lines of each slot. The interrupt priorisation will be managed by the 7 level VMEbus interrupt structure. Interrupt sources on the same level are processed by an onboard round robin scheduler. The strobe function of each slot and the state of four optional LED's located on the front can be controlled by the board control register of the **IPC03**.

All power supply lines of each slot are equipped with a LC filter for proper EMI protection. In addition, the 5 volt power supply line of each slot is short circuit protected by a 2AT fuse to avoid board and/or connector destruction in case of a short circuit of the usually high rated 5 volt power supply. The fuse condition as well as the IP-Error line of each slot can be checked within the system buffer of the **IPC03**. The +/-12 volt lines are not fused, because of the usually smaller dimensioned 12 volt power supply. All slot lines, which are not used or work as input to the **IPC03**, are tied to a high level by 10K pull-up resistor.

The **IPC03** memory access is performed within the VMEbus standard access area. All other accesses are handled within the VMEbus short I/O decoding range. The standard access base address and range can be enabled and adjusted by software. The short I/O access base address can be set by a four bit hex-code switch in 4 KByte steps.

The **IPC03** offers two different hardware timing modes, the 2 cycle and the 3 cycle select sequence, which can be dynamically enabled or disabled by software. This allows the use of any IP-modules, independent of their select and termination capabilities.

The VMEbus interface of the **IPC03** conforms to the specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The 5 volt board supply voltage is protected by a transient suppressor diode against overvoltage or wrong polarity. The **IPC03** PCB consists of four signal and two power supply planes to satisfy for proper EMV conformance.

1.2 Options

- IP-Modules according to Green Spring Logic Interface Specification Rev.0.7.1

1.3 Specifications

The power requirements for the **IPC03** carrier board are shown in the following table.
The power consumption of the used IP-Modules must be added to the given values.
The 5 volt supply of each IP-Slot is limited to 2 amp. max. by the onboard fuses.

- **Power Requirements:**

+5V,	+0.25V	-0.125V	0,5A + X
+12V,	+0.60V	-0.36V	0mA + Y
-12V,	-0.60V	+0.36V	0mA + Z

(X,Y,Z refer to additional power consumption of the used piggybacks)

- **Environmental Requirements**:

Operating Temperature	-40 degrees C to + 85 ° C
Relative Humidity	0 to 95% (non-condensing)
Storage Temperature	-40 °C to +85 °C

- **Board Dimensions:**

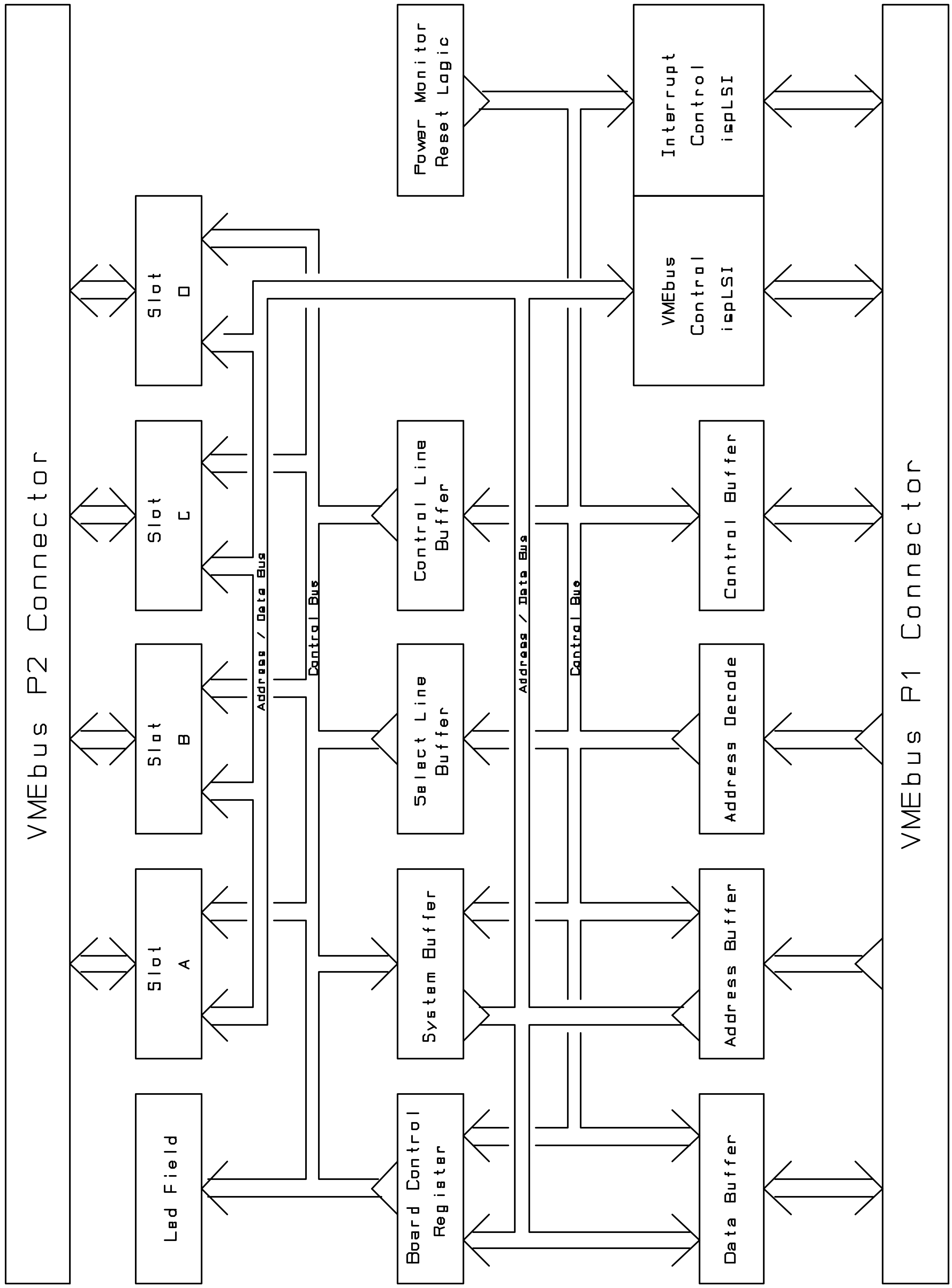
Double Euro Format:	Length: 233,4 mm
	Width: 160 mm

1.4 Related Documentation

The following manuals are applicable to the IPC03:

- VMEbus Specification Manual ANSI/IEEE STD1014-1987
- Green Spring IndustryPack Logic Interface Specification

1.5 IPC03 Block Diagram


VMEbus P2 Connector
Slot D
Slot C
Slot B
Slot A
Led Field
Address / Data Bus
Control Bus
Power Monitor
Reset Logic
Control Line Buffer
Select Line Buffer
System Buffer
Board Control Register
Address / Data Bus
Control Bus
Interrupt Control impLSI
VMEbus Control impLSI
Control Buffer
Address Decode
Address Buffer
Data Buffer
VMEbus P1 Connector

2. Delivery

2.1 The following items are shipped with this unit

- User's Manual IPC03
- MicroSys shipping carton

ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys Shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for IPC03 installation

For installation of the **IPC03**, the following items are required.

- Card cage or housing
- VMEbus motherboard
- Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +5V (+5 %, -2,5 %).
- mounted IP-Modules may require +/-12V.
- Be sure voltage is of correct polarity.
- Unit should only be inserted into, and removed from card cage when power is off.
- The IP-Modules must only be inserted or removed during power off.
- The card cage should be well ventilated. The operating temperature should never exceed it's specified range.
- Check default jumper or switch setting.

GUARANTEE IS VOID IF UNIT IS OPERATED OUT OF IT'S SPECIFICATIONS!

4. Board Overview

4.1 Features IPC03

- double eurocard format
- four onboard IP-Slots
- D8/D16 memory cycle support
- D8/D16 I/O cycle support
- 4/2/1/0.5 MByte programmable memory address space
- 128 Byte I/O address space
- 32 Byte ID read cycle support
- 8 x 7 level & vector programmable VMEbus interrupter
- 8 input round robin interrupt scheduler for 4 IP-Slots
- IP-Strobe function for each slot by read/write register
- IP-Error detection for each slot by read only register
- IP-Fuse fault detection for each slot by read only register
- programmable VMEbus standard access address
- hex-code switch for VMEbus short I/O base access address
- programmable two or three cycle select mode support
- fuse protection for 5 volt supply of each IP-Slot
- EMI filter protection for all supply lines of each IP-Slot
- separated shield layer underneath each IP module area
- ground & Vcc layer on logic area for proper EMV conformance
- very low component mounting hight underneath IP module area
- VMEbus A16/A24, D8/D16 slave board
- I/O interconnection according to VME64 specification
- conforms to VMEbus specification ANSI/IEEE STD1014-1987

5. VMEbus Address Map IPC03

5.1 VMEbus Short I/O Access Address Selection:

Switch Position	VMEbus Access Address
0	$0000 - $0FFF
1	$1000 - $1FFF
2	$2000 - $2FFF
3	$3000 - $3FFF
4	$4000 - $4FFF
5	$5000 - $5FFF
6	$6000 - $6FFF
7	$7000 - $7FFF
8	$8000 - $8FFF
9	$9000 - $9FFF
A	$A000 - $AFFF
B	$B000 - $BFFF
C	$C000 - $CFFF
D	$D000 - $DFFF
E	$E000 - $EFFF
F	$F000 - $FFFF

5.2 VMEbus Short I/O Address Map:

interrupt level register IP-A	$x101 - $x101	D1-D3,D5-D7 read/write
interrupt level register IP-B	$x103 - $x103	D1-D3,D5-D7 read/write
interrupt level register IP-C	$x105 - $x105	D1-D3,D5-D7 read/write
interrupt level register IP-D	$x107 - $x107	D1-D3,D5-D7 read/write
board system buffer	$x108 - $x108	D8-D15 read only
board control register	$x10D - $x10D	D0-D7 read/write
strobe enable register	$x10F - $x10F	D1,D3,D5,D7 read/write
select acknowledge mode	$x180 - $1FF	read/write - disable/enable
VME address compare register 0	$x200 - $x27F	D0-D3 read/write
VME address mask register 0	$x200 - $x27F	D4-D7 read/write
VME address compare register 1	$x280 - $x2FF	D0-D1 read/write
VME address mask register 1	$x280 - $x2FF	D4-D5 read/write
VME standard access enable	$x300 - $x37F	read/write - disable/enable
select cycle mode	$x380 - $x3FF	read/write - disable/enable
IP-Module A IO-Select	$x400 - $x47F	D0-D15 read/write
IP-Module A ID-Select	$x480 - $x4FF	D0-D15 read/write
IP-Module B IO-Select	$x500 - $x57F	D0-D15 read/write
IP-Module B ID-Select	$x580 - $x5FF	D0-D15 read/write
IP-Module C IO-Select	$x600 - $x67F	D0-D15 read/write
IP-Module C ID-Select	$x680 - $x6FF	D0-D15 read/write
IP-Module D IO-Select	$x700 - $x77F	D0-D15 read/write
IP-Module D ID-Select	$x780 - $x7FF	D0-D15 read/write

5.3 VMEbus Standard Access Address Map:

The VMEbus address lines A19 to A23 are freely programmable. All lines from A19 to A23 can be individually masked. According to the masked address lines, different access ranges from 512KByte up to 4MByte for each slot can be arranged. The resulting base address must be added to the following values. A logical one masks the according VMEbus address line and it will not be used for address decoding.

Compare & Mask Register 0 Contents:	0 - 0 - 1 - 1 - x - x - x - x	
Compare & Mask Register 1 Contents:	x - x - x - 0 - x - x - x - x	
IP-Module A Memory Select	$00000000 - $0007FFFF	512KByte Range
IP-Module B Memory Select	$00080000 - $000FFFFF	512KByte Range
IP-Module C Memory Select	$00100000 - $0017FFFF	512KByte Range
IP-Module D Memory Select	$00180000 - $001FFFFF	512KByte Range

Compare & Mask Register 0 Contents:	0 - 1 - 1 - 1 - x - x - x - x	
Compare & Mask Register 1 Contents:	x - x - x - 0 - x - x - x - x	
IP-Module A Memory Select	$00000000 - $000FFFFF	1MByte Range
IP-Module B Memory Select	$00100000 - $001FFFFF	1MByte Range
IP-Module C Memory Select	$00200000 - $002FFFFF	1MByte Range
IP-Module D Memory Select	$00300000 - $003FFFFF	1MByte Range

Compare & Mask Register 0 Contents:	1 - 1 - 1 - 1 - x - x - x - x	
Compare & Mask Register 1 Contents:	x - x - x - 0 - x - x - x - x	
IP-Module A Memory Select	$00000000 - $001FFFFF	2MByte Range
IP-Module B Memory Select	$00200000 - $003FFFFF	2MByte Range
IP-Module C Memory Select	$00400000 - $005FFFFF	2MByte Range
IP-Module D Memory Select	$00600000 - $007FFFFF	2MByte Range

Compare & Mask Register 0 Contents:	1 - 1 - 1 - 1 - x - x - x - x	
Compare & Mask Register 1 Contents:	x - x - x - 1 - x - x - x - x	
IP-Module A Memory Select	$00000000 - $003FFFFF	4MByte Range
IP-Module B Memory Select	$00400000 - $007FFFFF	4MByte Range
IP-Module C Memory Select	$00800000 - $00BFFFFF	4MByte Range
IP-Module D Memory Select	$00C00000 - $00FFFFFF	4MByte Range

6. The IP-Slots A, B, C & D:

The **IPC03** offers four slots to carry either four single high or two double high modules. The 50 pin DSUB connector ST3 supplies module A with all necessary logic signals, while the modules B, C and D use ST5, ST7 and ST9. The opposite DSUB connectors ST4, ST6, ST8 and ST10 contain the I/O interface signals.

Each slot is equipped with a fused 5 volt and a non fused +/-12 volt supply. The soldered ‘picofuse’ is rated for 2AT and should only be replaced by the same kind and type. The fuse condition for each slot can be checked within the system buffer located at $x108 on the data lines D8 to D11 for slot A to slot D. The according data bit will be in a high state if the fuse is intact.

The component mounting hight underneath the IP module area is realized below 3mm (0.11inch) to allow for a good air flow between the carrier board and the I-Packs. The component free area underneath each slot contains a separate copper layer for enhanced noise protection. Each layer can be inductive, capacitiv or resistiv connected to the logic ground of the **IPC03** or left floating. A 3mm (0.11 inch) wide routing gap allows for a proper galvanic isolation.

Each slot is supplied with ID-, I/O- and memory select lines. All signals concerning the DMA controlled cycles are not used and tied to a logical high by pull-up resistors. The reserved pins of all slots are individually tied to high by pull-up resistors.

The strobe lines of the four slots, PSTRBA/B/C/D, are not bussed and can be accessed via the (B)oard (C)ontrol (R)egister, located at $x10C and the (S)trobe (E)nable (R)egister at $x10E within the VMEbus short I/O range. The value of the VMEbus data line D4 will cause the state of the PSTRBA line. The data lines D5, D6 and D7 control the PSTRBB, PSTRBC and PSTRBD lines, if the according enable bit within the SER is set to one. If the enable bit is set to zero, the according strobe line is tristated and can be driven by the IP module. The enable bits are located on the data lines D1, D3, D5 and D7 for the strobe lines of slot A, B, C, and D. The remaining data lines of the lower byte of the BCR from D0 to D3 are used to handle the four user leds A, B, C and D on the frontpanel.

The state of the four error lines, PERRA*, PERRB*, PERRC* and PERRD* will be reflected within the upper byte of the system buffer located at $x108 within the VMEbus short I/O range. The state of the slot A error line will be reflected on data line D12, while slot B, C and D use the data lines D13, D14 and D15. The error lines are tied to a logical high if they are not driven by an IP module. The remaining data lines from D8 to D11 are used for the fuse condition detection of the four IP slots. The lower byte from D0 to D7 is not used and may have any state during read operations.

6.1 System Buffer Register:

$x108	D15	D14	D13	D12	D11	D10	D9	D8
slot:	D	C	B	A	D	C	B	A
fuse A O.K.	x	x	x	x	x	x	x	1
fuse A blown	x	x	x	x	x	x	x	0
fuse B O.K.	x	x	x	x	x	x	1	x
fuse B blown	x	x	x	x	x	x	0	x
fuse C O.K.	x	x	x	x	x	1	x	x
fuse C blown	x	x	x	x	x	0	x	x
fuse D O.K.	x	x	x	x	1	x	x	x
fuse D blown	x	x	x	x	0	x	x	x
Error-Line-A	x	x	x	state	x	x	x	x
Error-Line-B	x	x	state	x	x	x	x	x
Error-Line-C	x	state	x	x	x	x	x	x
Error-Line-D	state	x	x	x	x	x	x	x

6.2 Board Control Register:

$x10D	D7	D6	D5	D4	D3	D2	D1	D0
reset state	0	0	0	0	0	0	0	0
user led A on	x	x	x	x	x	x	x	1
user led B on	x	x	x	x	x	x	1	x
user led C on	x	x	x	x	x	1	x	x
user led D on	x	x	x	x	1	x	x	x
strobe line A	x	x	x	state	x	x	x	x
strobe line B	x	x	state	x	x	x	x	x
strobe line C	x	state	x	x	x	x	x	x
strobe line D	state	x	x	x	x	x	x	x

6.3 Strobe Enable Register:

$x10F	D7	D6	D5	D4	D3	D2	D1	D0
reset state	0	0	0	x	0	0	0	x
strobe line A tristate	x	x	x	x	x	x	0	x
strobe line A totem pole	x	x	x	x	x	x	1	x
strobe line B tristate	x	x	x	x	0	x	x	x
strobe line B totem pole	x	x	x	x	1	x	x	x
strobe line C tristate	x	x	0	x	x	x	x	x
strobe line C totem pole	x	x	1	x	x	x	x	x
strobe line D tristate	0	x	x	x	x	x	x	x
strobe line D totem pole	1	x	x	x	x	x	x	x

6.4 Pin assignment of the logical interface connectors ST3, ST5, ST7 and ST9:

DSUB Connector Pin:		Signal Name:	
1	26	Ground	Ground
2	27	CLOCK	+5V/2A
3	28	RESET	R/W*
4	29	D0	ID-Select*
5	30	D1	(DMA-Request0*)
6	31	D2	Memory-Select*
7	32	D3	(DMA-Request1*)
8	33	D4	Int.-Select*
9	34	D5	(DMA-Acknowledge*)
10	35	D6	I/O-Select*
11	36	D7	(reserved 0)
12	37	D8	A1
13	38	D9	(DMA-End*)
14	39	D10	A2
15	40	D11	Error*
16	41	D12	A3
17	42	D13	IRQ0*
18	43	D14	A4
19	44	D15	IRQ1*
20	45	LDS*	A5
21	46	UDS*	Strobe
22	47	-12V	A6
23	48	+12V	Acknowledge*
24	49	+5V/2A	(reserved 1)
25	50	Ground	Ground

Signals within brackets are not used !

An '*' indicates a low active signal.

7. The IP I/O-VMEbus Signal Mapping

The IPC03 features the VME64x interconnection standard for IP carriers to the VME-ST0 and VME-ST2 connectors. The female ST0 connector contains 6 rows of 19 pins, which allows for 95 I/O signals and 19 ground pins. The male 192 pin ST2 connector uses the rows A, C, D and Z for the I/O signal mapping, while row C is only used for ground and power supply connections.

7.1 Pin Assignment of the VMEbus Connector ST0:

Pin	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	D5	D4	D3	D2	D1
2	GND	D10	D9	D8	D7	D6
3	GND	D15	D14	D13	D12	D11
4	GND	D20	D19	D18	D17	D16
5	GND	D25	D24	D23	D22	D21
6	GND	D30	D29	D28	D27	D26
7	GND	D35	D34	D33	D32	D31
8	GND	D40	D39	D38	D37	D36
9	GND	D45	D4	D4	D4	D41
10	GND	D50	D4	D4	D4	D46
11	GND	C5	C4	C3	C2	C1
12	GND	C10	C9	C8	C7	C6
13	GND	C15	C14	C13	C12	C11
14	GND	C20	C19	C18	C17	C16
15	GND	C25	C24	C23	C22	C21
16	GND	C30	C29	C28	C27	C26
17	GND	C35	C34	C33	C32	C31
18	GND	C40	C39	C38	C37	C36
19	GND	C45	C44	C43	C42	C41

7.2 Pin Assignment of the VMEbus Connector ST2:

Pin	Row Z	Row A	Row B	Row C	Row D
1	C46	B41	+5V	B42	C47
2	GND	B43	GND	B44	C48
3	C49	B45	n.c.	B46	C50
4	GND	B47	n.c.	B48	B1
5	B2	B49	n.c.	B50	B3
6	GND	A1	n.c.	A2	B4
7	B5	A3	n.c.	A4	B6
8	GND	A5	n.c.	A6	B7
9	B8	A7	n.c.	A8	B9
10	GND	A9	n.c.	A10	B10
11	B11	A11	n.c.	A12	B12
12	GND	A13	GND	A14	B13
13	B14	A15	+5V	A16	B15
14	GND	A17	n.c.	A18	B16
15	B17	A19	n.c.	A20	B18
16	GND	A21	n.c.	A22	B19
17	B20	A23	n.c.	A24	B21
18	GND	A25	n.c.	A26	B22
19	B23	A27	n.c.	A28	B24
20	GND	A29	n.c.	A30	B25
21	B26	A31	n.c.	A32	B27
22	GND	A33	GND	A34	B28
23	B29	A35	n.c.	A36	B30
24	GND	A37	n.c.	A38	B31
25	B32	A39	n.c.	A40	B33
26	GND	A41	n.c.	A42	B34
27	B35	A43	n.c.	A44	B36
28	GND	A45	n.c.	A46	B37
29	B38	A47	n.c.	A48	B39
30	GND	A49	n.c.	A50	B40
31	n.c.	n.c.	GND	n.c.	GND
32	GND	n.c.	+5V	n.c.	+5V

8. The Standard Access Address Programming

The memory select line of each of the four IP modules requires according to specification 8MBytes addressing range. This would cause a single carrier board with two I-Packs to cover the whole standard VMEbus addressing range. Usually, only a small part or no memory select at all is used onboard most of the IP modules. Therefore, the address decoding range of the memory select area can be programmed onboard the **IPC03** within two registers. The state of the VMEbus address lines from A19 to A23 is compared to the contents of the two address compare registers at location $x201 and $x281, and, if the according mask bits are set to zero, used for decoding. After a reset, the standard address decoding is disabled at all, to avoid an unintended interference of the **IPC03** during initialization and ram search procedures usually executed after power up. The standard address range is enabled by a write access to the address location $x300. A read access to this location disables the standard access range. For any access within the memory select range, the proper VMEbus address modifier combination must be asserted by the accessing VMEbus master.

8.1 VMEbus address modifier bit map:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	H	H	L	Standard Supervisory Prog.	(3E)
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	H	L	Standard User Prog.	(3A)
H	H	H	L	L	H	Standard User Data	(39)

L = logical low H = logical high

8.2 VME Compare and Mask Register 0:

D7	D6	D5	D4	D3	D2	D1	D0
Mask VME				Compare VME			
A22	A21	A20	A19	A22	A21	A20	A19

8.3 VME Compare and Mask Register 1

D7	D6	D5	D4	D3	D2	D1	D0
Mask VME				Compare VME			
not used	not used	not used	A23	not used	not used	not used	A23

8.4 The VMEbus standard access address programming procedure:

(e.g. access address $400000, 1MByte/Slot, code switch position 7)

1.) set the compare and mask register for VMEbus address line A19 to A22 by a byte write access to the short I/O location $x201.

```
move.b #$78,$7201   :   - mask A19, A20, A21
                        - don't mask A22
                        - compare A22 to high
```

2.) set the compare and mask register for VMEbus address line A23 by a byte write access to the short I/O location $x281.

```
move.b #$00,$7281   :   - don't mask A23
                        - compare A23 to low
```

3.) set the VMEbus standard access enable bit by a write command to the short I/O location $x300.

```
move.w #$0,$7300
```

4.) now, the memory select range for:

module A reaches from $400000 to $4FFFFF
module B reaches from $500000 to $5FFFFF
module C reaches from $600000 to $6FFFFF
module D reaches from $700000 to $7FFFFF

Attention !
The IPC 03 does not accept longword accesses within the standard access address range !

9. The IP module IO and ID select access

The **IPC03** uses the VMEbus short I/O access range to decode the IO and ID select lines for the four IP slots. The onboard code switch allows for 16 possible base address configurations in
4 KByte steps starting at $0000. The VMEbus address modifier combination $29 or $2D must be supplied during the access of a VMEbus master board for this address range. This addressing scheme is fixed by hardware and cannot be modified or disabled.

9.1 VMEbus address modifier bit map:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low   H = logical high

The ID select address of each slot is always decoded with an address offset of $80 to its IO decoding range. The IO select base address of slot A is set to $x400, that of slot B, C and D are $x500, $x600 and $x700. The decoding range of both cycle types is $7F wide and read as well as write accesses are allowed on both, however the data buffers are not activated during writes to the ID select range.

9.2 The IO and ID select address map:

IP-Module A IO-Select	$x400 - $x47F	D0-D15 read/write
IP-Module A ID-Select	$x480 - $x4FF	D0-D15 read/write
IP-Module B IO-Select	$x500 - $x57F	D0-D15 read/write
IP-Module B ID-Select	$x580 - $x5FF	D0-D15 read/write
IP-Module C IO-Select	$x600 - $x67F	D0-D15 read/write
IP-Module C ID-Select	$x680 - $x6FF	D0-D15 read/write
IP-Module D IO-Select	$x700 - $x77F	D0-D15 read/write
IP-Module D ID-Select	$x780 - $x7FF	D0-D15 read/write

10. Board specific parameters

The VMEbus 'LDS' data strobe line controlling the VMEbus data lines D0 to D7 activates the IP slot byte select line for the IP slot data lines D0 to D7. The VMEbus 'UDS' data strobe line controls the remaining data lines D8 to D15.

As a standard access timing for the any cycle type, the 3 clock sequence is implemented within the on board VME ispLSI. The 2 clock sequence can be activated by software, but the user should verify, that the used IP modules are able to work in this fast termination mode.

After a reset, the standard 3 cycle mode is enabled. The 2 cycle mode can be set by a write access to the address offset location $x380. The return to the 3 cycle mode is performed by a read access of location $x380.

Clock Mode Switch

Access Address	Access Mode	Function
$X380	byte or word read	set 3 clock mode
$X380	byte or word write	set 2 clock mode

10.1 The 3 clock access timing:

1.)	clock speed:	8 MHz / 125ns	
2.)	select phase:	activated signals:	select line address lines A1-A22 byte select lines read/write line data on write cycles
3.)	hold phase:	deactivated signals: check and wait for:	address lines A7-A22 acknowledge line active
4.)	terminate phase:	deactivated signals:	select line address lines A1 - A6 byte select lines read/write line data on write cycles

10.2 The 2 clock access timing:

1.)	clock speed:	8MHz / 125ns	
2.)	select phase:	activated signals:	select line
			address lines A1-A22 byte select lines read/write line data on write cycles
3.)	terminate phase:	deactivated signals: check and wait for: then deactivate	select line address lines A7-A22 acknowledge line active address lines A1 - A6 byte select lines read/write line data on write cycles

Because of a definition gap within the IP specification, an additional feature is added to the IP control interface of the **IPC 03**. According to the IP specification, any module may hold its acknowledge line contiguously active. This fact would cause either an interlock or an erroneous data transfer if the release of the according IP acknowledge line is checked or not, before asserting one of its select lines. For this case, the user can configure the IP slot controller via a software switch for one of these modes. After a reset, the acknowledge release check is enabled, and a module, contiguous asserting its acknowledge line would lock both IP slots after the first access and any further access will be abnormally terminated by the onboard bus monitor. The acknowledge check can be disabled by a byte or word sized write access to the address offset location $x180. In this case, the acknowledge line is only checked during an active slot cycle and it will be ignored after the cycle has been terminated and all select and strobe lines of the IP slots have reached the inactive state. This mode may cause wrong data to be transferred if it is used together with IP modules which are deasserting their acknowledge line during inactive states and have asserted their acknowledge line for more the 2 clock cycles during active states. In this case a fast consecutive IP access cycle may still detect the previous asserted acknowledge line active and terminate the current access.

Acknowledge Mode Switch

Access Address	Access Mode	Function
$x180	byte or word read	set acknowledge release mode check
$x180	byte or word write	set contiguous acknowledge mode

11. The VMEbus Interrupter:

The **IPC03** is equipped with eight programmable 7 level VMEbus interrupters. The access range of its registers reaches within the VMEbus short I/O range from $x101 up to $x107 as an address offset to the selectable board base address. The desired level for each interrupt source can be loaded into its interrupt level register. The interrupt vector must be supplied by the according IPModule. The eight interrupt sources from the four possible IP modules may have any level combination. If several sources share the same level, the according acknowledge will be preprocessed by a round robin scheduler to guarantee a fair interrupt handling and to avoid the level to be blocked by a contiguous asserted request. The eight level registers are cleared by any reset, i.e. level 0 is programmed for each source, which will cause any IP module interrupt to be disabled. Each level register is 3 bits wide and use either the data lines D1 to D3 or D5 to D7. The data lines D0 and D4 are not used within the interrupt level registers and may have any value. The register contents can be read back for verification.

11.1 Address map of the interrupt level registers:

$x101	D1-D3	module A	irq 0	byte read/write
$x101	D5-D7	module A	irq 1	byte read/write
$x103	D1-D3	module B	irq 0	byte read/write
$x103	D5-D7	module B	irq 1	byte read/write
$x105	D1-D3	module C	irq 0	byte read/write
$x105	D5-D7	module C	irq 1	byte read/write
$x107	D1-D3	module D	irq 0	byte read/write
$x107	D5-D7	module D	irq 1	byte read/write

The upper byte of the given access addresses is not used and may have any value. The interrupt level registers can be modified via odd byte or even aligned word accesses.

11.2 Bit map of the VMEbus interrupt level for any module:

	IRQ Line 1				IRQ Line 0			
Data Line	D7	D6	D5	D4	D3	D2	D1	D0
disable	0	0	0	x	0	0	0	x
Level 1	0	0	1	x	0	0	1	x
Level 2	0	1	0	x	0	1	0	x
Level 3	0	1	1	x	0	1	1	x
Level 4	1	0	0	x	1	0	0	x
Level 5	1	0	1	x	1	0	1	x
Level 6	1	1	0	x	1	1	0	x
Level 7	1	1	1	x	1	1	1	x

(x = don't care)

12. The Board Control Register:

The **IPC03** contains a 8 bit wide read/write control register for board maintenance. The access address is located within the VMEbus short I/O range with an address offset of $x10D to the selectable board base address.
The user leds will be activated if the according data lines of the BCR are set to a low state. The state of data line D0 controls user led A, while D1 to D3 are used for the user leds B, C and D. The strobe line for slot A is handled by the state of data line D4. Slot B, C and D use the according data lines D5, D6 and D7.
The BCR can be read back for verification. After a power up reset, the contents of the BCR is not defined and may have any value. However, the BCR will be disabled by any reset and all lines are set to high, to avoid an undefined and/or unintended addressing mode. After the first write operation to the BCR, it will be enabled automatically and its contents will be able to affect the **IPC03** board functions. A read access will not affect the disabled state of the BCR.

12.1 Bitmap of the Board Control Register:

D0	User Led A	low active
D1	User Led B	low active
D2	User Led C	low active
D3	User Led D	low active
D4	Strobe Line Module A	module dependent
D5	Strobe Line Module B	module dependent
D6	Strobe Line Module C	module dependent
D7	Strobe Line Module D	module dependent

13. The Strobe Enable Register:

The **IPC03** is able to control the state of each of the four IP module specific strobe lines. The state control contains high, low or tristate, in case the line will be driven by the IP module. After a reset the strobe drivers are disabled and set to tristate mode. If the strobe line is set to totem pole, the state of the according BCR bit will be driven by the strobe line buffer..

13.1 Bitmap of the Strobe Enable Register:

$x10F	D7	D6	D5	D4	D3	D2	D1	D0
reset state	0	0	0	x	0	0	0	x
strobe line A tristate	x	x	x	x	x	x	0	x
strobe line A totem pole	x	x	x	x	x	x	1	x
strobe line B tristate	x	x	x	x	0	x	x	x
strobe line B totem pole	x	x	x	x	1	x	x	x
strobe line C tristate	x	x	0	x	x	x	x	x
strobe line C totem pole	x	x	1	x	x	x	x	x
strobe line D tristate	0	x	x	x	x	x	x	x
strobe line D totem pole	1	x	x	x	x	x	x	x

14. The System Buffer:

The **IPC03** offers an 8 bit wide read only system buffer to reflect some status information about the module and slot condition. It is located at the VMEbus short I/O access address offset $x108 on the upper data byte lines D8 to D15. It contains the four module specific error lines and the four fuse condition signals about the 5 volt supply voltage of each slot. The 12 volt supply is not fused and does not affect the system buffer. The system buffer will only respond on even aligned byte or word read accesses. All other access types will not return valid data, but cause no operation or no damage. Any write access will be accepted but has not affect to the system buffer.

14.1 Bitmap of the System Buffer:

D0-D7	not used	any state
D8	5V fuse of module A	high if intact
D9	5V fuse of module B	high if intact
D10	5V fuse of module C	high if intact
D11	5V fuse of module D	high if intact
D12	error line of module A	module dependent
D13	error line of module B	module dependent
D14	error line of module C	module dependent
D15	error line of module D	module dependent

15. The VMEbus Interface

The bus interface of the **IPC03** is designed according to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The VMEbus connector ST1 contains on the row A, B and C all standard VMEbus lines, necessary for A16/A24, D8/D16 slave boards. The VMEbus connector ST2 contains the recommended VME64x signal mapping for the IP slot I/O interface signals. It contains 192 pins in 5 rows with I/O signals on the rows A, C, D and Z. The row B is used only for additional ground and power supply connections. The remaining 95 IP slot interface signals are connected to the VMEbus connector ST0. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals AM0 to AM5 are a part of the VMEbus specifications and serve to differentiate between certain memory areas. With the exception of the AM2 line, all other lines are used for the onboard decoding logic. The **IPC03** accepts accesses within the VMEbus short I/O range, the VMEbus standard access area and the VMEbus extended addressing range.

15.1 The following AM-Codes are accepted by the IPC03:

AM5	AM4	AM3	AM2	AM1	AM0	Access for:	
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)
L	L	H	H	L	H	Extended Supervisory Data	(0D)
L	L	H	L	L	H	Extended User Data	(09)

L = logical low H = logical high

15.2 Pin Assignment of the VMEbus Connector ST0:

Pin	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	D5	D4	D3	D2	D1
2	GND	D10	D9	D8	D7	D6
3	GND	D15	D14	D13	D12	D11
4	GND	D20	D19	D18	D17	D16
5	GND	D25	D24	D23	D22	D21
6	GND	D30	D29	D28	D27	D26
7	GND	D35	D34	D33	D32	D31
8	GND	D40	D39	D38	D37	D36
9	GND	D45	D4	D4	D4	D41
10	GND	D50	D4	D4	D4	D46
11	GND	C5	C4	C3	C2	C1
12	GND	C10	C9	C8	C7	C6
13	GND	C15	C14	C13	C12	C11
14	GND	C20	C19	C18	C17	C16
15	GND	C25	C24	C23	C22	C21
16	GND	C30	C29	C28	C27	C26
17	GND	C35	C34	C33	C32	C31
18	GND	C40	C39	C38	C37	C36
19	GND	C45	C44	C43	C42	C41

15.3 Pin Assignment of the VMEbus Connector ST1:

Pin	Row A	Row B	Row C
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	(SYSCLK)	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	UDS*	(BR0*)	SYSRESET*
13	LDS*	(BR1*)	LWORD*
14	RW*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	(AM2)	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	——	A17
22	IACKOUT*	——	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	(5VSTB)	+12V
32	+5V	+5V	+5V

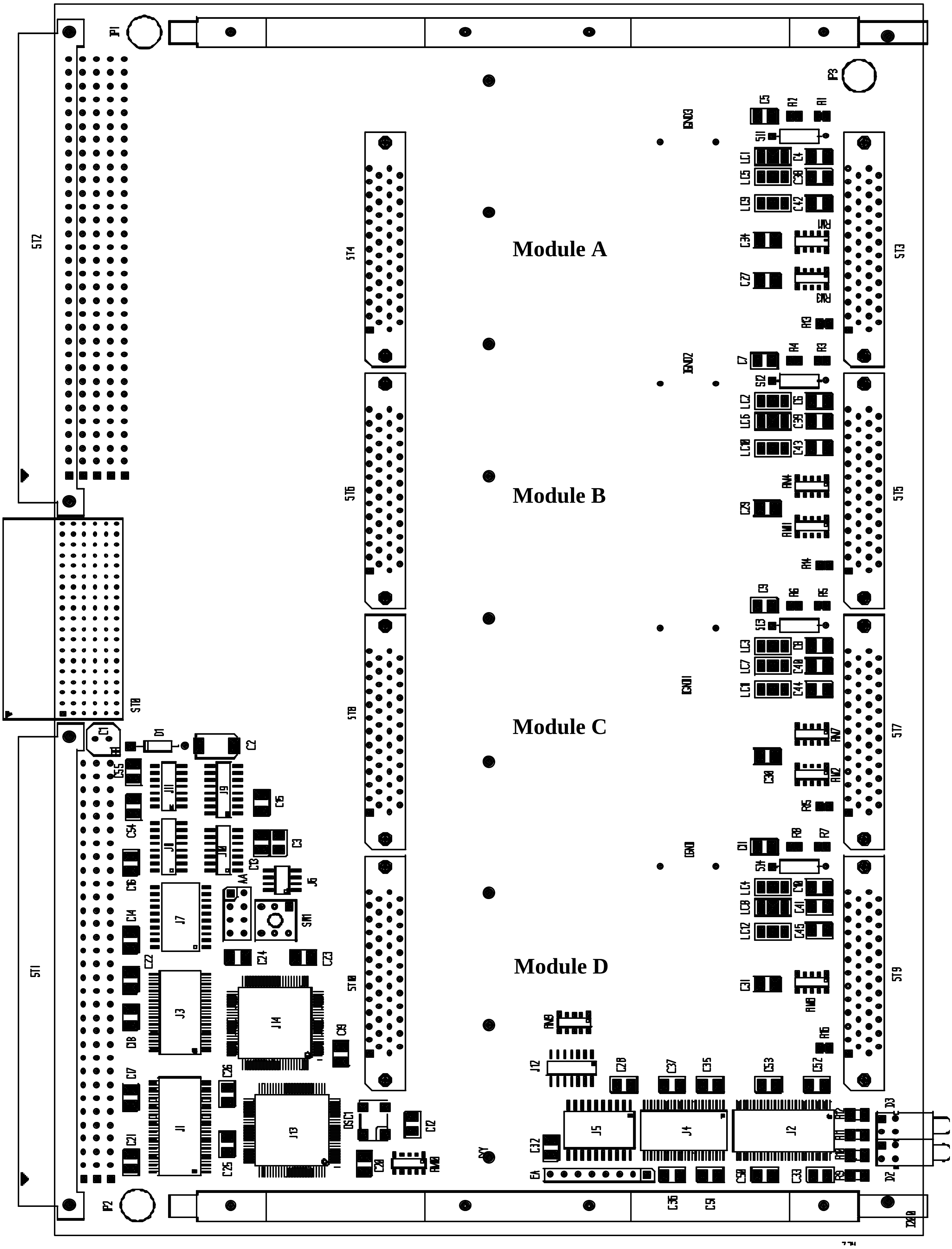
(signals within brackets are not used or connected)

15.4 Pin Assignment of the VMEbus Connector ST2:

Pin	Row Z	Row A	Row B	Row C	Row D
1	C46	B41	+5V	B42	C47
2	GND	B43	GND	B44	C48
3	C49	B45	n.c.	B46	C50
4	GND	B47	n.c.	B48	B1
5	B2	B49	n.c.	B50	B3
6	GND	A1	n.c.	A2	B4
7	B5	A3	n.c.	A4	B6
8	GND	A5	n.c.	A6	B7
9	B8	A7	n.c.	A8	B9
10	GND	A9	n.c.	A10	B10
11	B11	A11	n.c.	A12	B12
12	GND	A13	GND	A14	B13
13	B14	A15	+5V	A16	B15
14	GND	A17	n.c.	A18	B16
15	B17	A19	n.c.	A20	B18
16	GND	A21	n.c.	A22	B19
17	B20	A23	n.c.	A24	B21
18	GND	A25	n.c.	A26	B22
19	B23	A27	n.c.	A28	B24
20	GND	A29	n.c.	A30	B25
21	B26	A31	n.c.	A32	B27
22	GND	A33	GND	A34	B28
23	B29	A35	n.c.	A36	B30
24	GND	A37	n.c.	A38	B31
25	B32	A39	n.c.	A40	B33
26	GND	A41	n.c.	A42	B34
27	B35	A43	n.c.	A44	B36
28	GND	A45	n.c.	A46	B37
29	B38	A47	n.c.	A48	B39
30	GND	A49	n.c.	A50	B40
31	n.c.	n.c.	GND	n.c.	GND
32	GND	n.c.	+5V	n.c.	+5V

Appendices

Appendix A: Layout Component Side



Appendix B: Schematics