Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
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Germany

declare that the product

IP 003 / IE 003

is in conformity with:

EN 50081-1	**Generic emission standard**
EN 50082-1	**Generic immunity standard**

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date: 08.04.97

Signature:

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User's Manual

IP 003 / IE 003

5th edition

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1. Introduction

1.1 Short Description

The IP003 is a single height board out of the MicroSys VMEbus line. It is used as a non intelligent carrier board for upto four ‘IndustryPack‘ modules according to the Green Spring Logic Interface Specification Revision 0.7.1 for IP-Modules. Two modules can be mounted directly onto the IP003, for the other two modules, a piggyback extention board (IE003) must be used. The front end of the IP-Module slots can be equipped with different adapter boards of the IPAxx series. The IP003 supports all kind of single or double IP-Modules with an 8 or 16 bit wide data bus. The module clock rate is fixed to 8 MHz. Non DMA IO- and Memory-Cycles are supported. All interrupt sources of each module slot are processed by a programmable VMEbus interrupter with a round robin scheduler. The strobe function as well as the IP-Error input of each slot can be controlled by the IP003. The 5 volt power supply of each slot is short circuit protected by a 2AT fuse. The +/-12 volt lines are not fused. All slot lines, which are not used or work as input to the IP003, are tied to a high level by 10K pullup resistor networks. The IP003 memory access is performed within the VMEbus standard access area. All other accesses are handled within the VMEbus short I/O access range. The standard access base address and range is adjusted by software. The short I/O access base address is set by a four bit hex-code switch. The VMEbus interface of the IP003 conforms to the specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The 5 volt board supply voltage is protected by a transient suppressor diode.

1.2 Options

- IPA01 front end adapter board
- IE003 piggyback extention board with two IP-Slots
- IP-Modules according to Green Spring Logic Interface Specification Rev.0.7.1

1.3 Specifications

The power requirements for the IP003 carrier board are shown in the following table. The power consumption of the used IP-Modules must be added to the given values. The 5 volt supply of each IP-Slot is limited to 2A max. by the onboard fuses.

+5V, +/-5%,	0.3 A	
+12V, +/-10%,	0.0 A	(neccessary for IP-module only)
-12V, +/-10%,	0.0 A	(neccessary for IP-module only)

1.4 Related Documentation

The following manuals are applicable to the IP003

- VMEbus Specifiaction Manual ANSI/IEEE STD1014-1987
- Green Spring IndustryPack Logic Interface Specification

2. Delivery

2.1 Items shipped with this unit

- User's Manual IP003 / IE 003 Hardware
- MicroSys shipping carton

ATTENTION: STATIC DISCHARGE CAN DESTROY THIS UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys Shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for IP003 installation

For the installation of the IP003, the following items are required.

- Card Cage or housing
- VMEbus Motherboard
- VME master CPU
- Adequate rated power supply
- IP-module

3.2 Points to be observed

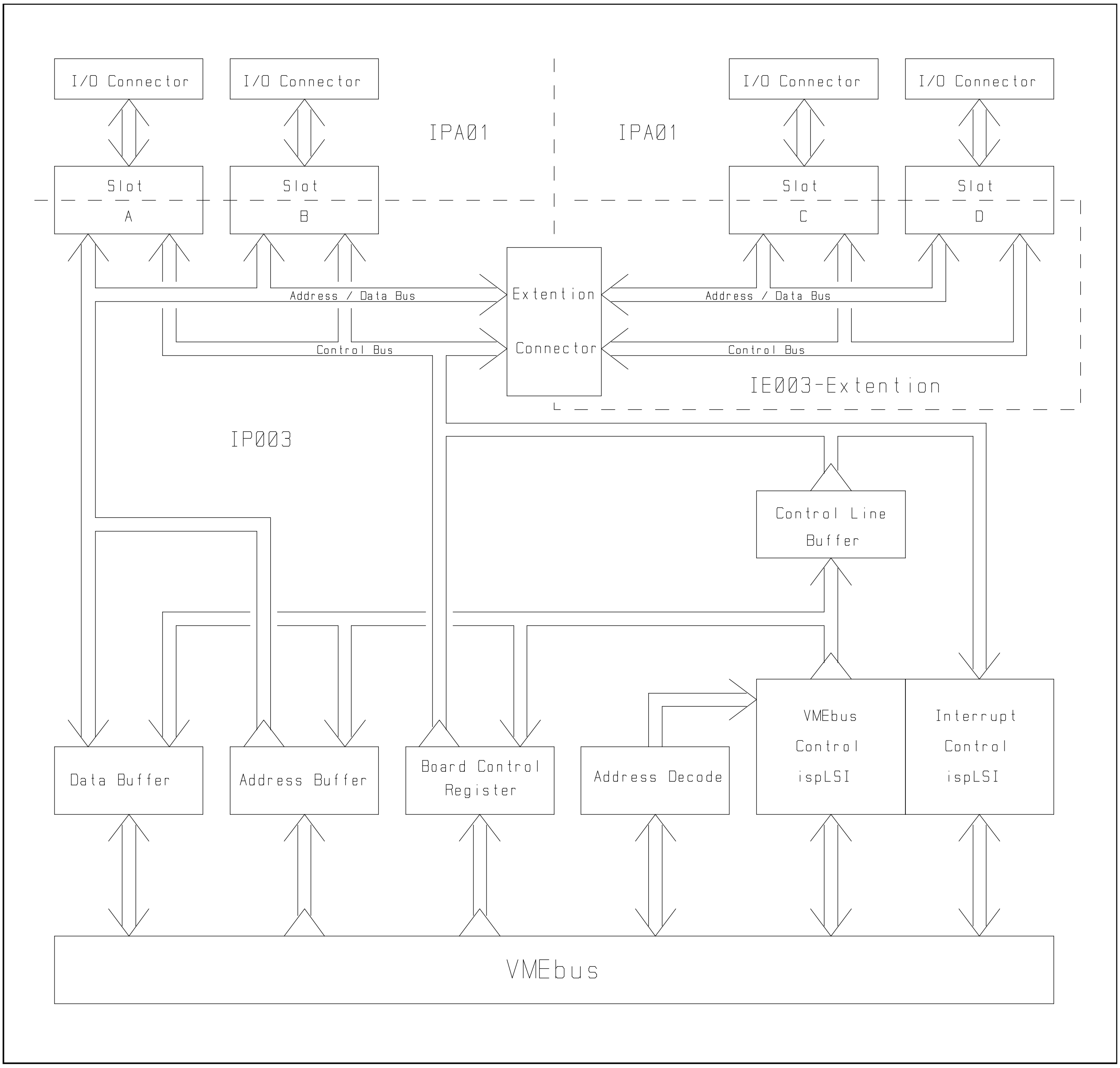
Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +5V (+5%, -2,5%)
- Be sure voltage is of correct polarity
- Unit should only be inserted into, and removed from card cage when power is off.
- The card cage should be well ventilated. The operating temperature should never exceed its specified range.
- Check default jumper setting

GUARANTEE IS VOID IF UNIT IS OPERATED OUT OF ITS SPECIFICATIONS

With the above points adhered to, the unit can be inserted into the card cage.

4. IP003 Block Diagram



5. IP003 Features

- single eurocard format
- two onboard IP-Slots
- extension bus for two piggyback IP-Slots
- 8/16 bit data memory cycle support
- 8/16 bit data I/O cycle support
- 2/1/0.5/0.25/0 MByte programmable memory address space
- 128 Byte I/O address space
- 32 Byte ID read cycle support
- 7 level & vector programmable VMEbus interrupter
- 8 input round robin interrupt scheduler for 4 IP-Slots
- IP-Strobe function for each slot by read/write register
- IP-Error detection for each slot by read only register
- programmable VMEbus standard access address
- hex-code switch for VMEbus short I/O access address
- fuse protection for 5 volt supply of each IP-Slot
- separated ground layer underneath IP module area
- ground & Vcc layer on logic area for proper EMV conformance
- very low component mounting height underneath IP module area
- exchangeable front end for I/O connector configuration
- works as VMEbus A16/A23, D8/D16 slave board
- conforms to VMEbus specification ANSI/IEEE STD1014-1987

6. Detailed Description

6.1 VMEbus Address Map IP003

VMEbus Short I/O Access Address Selection

Hex-Code Switch Position:	VMEbus Access Address:
0	$0000 - $0FFF
1	$1000 - $1FFF
2	$2000 - $2FFF
3	$3000 - $3FFF
4	$4000 - $4FFF
5	$5000 - $5FFF
6	$6000 - $6FFF
7	$7000 - $7FFF
8	$8000 - $8FFF
9	$9000 - $9FFF
A	$A000 - $AFFF
B	$B000 - $BFFF
C	$C000 - $CFFF
D	$D000 - $DFFF
E	$E000 - $EFFF
F	$F000 - $FFFF

VMEbus Short I/O Address Map

Shift Register Clear	$x000 - $x3FF	read only
Compare Shift Register Clock	$x000 - $x3FF	write only
Mask Shift Register Clock	$x400 - $x7FF	write only
Board Control Register	$x800 - $xBFF	read/write
IP-Module A ID Select	$xC00 - $xC7F	read only
IP-Module B ID Select	$xC80 - $xCFF	read only
IP-Module C ID Select	$xD00 - $xD7F	read only
IP-Module D ID Select	$xD80 - $xDFF	read only
IP-Module A I/O Select	$xE00 - $xE7F	read/write
IP-Module B I/O Select	$xE80 - $xEFF	read/write
IP-Module C I/O Select	$xF00 - $xF7F	read/write
IP-Module D I/O Select	$xF80 - $xFFF	read/write

VMEbus Standard Access Address Map

The VMEbus address lines A18 to A23 are programmable and maskable.
According to the masked address lines, different access ranges from 256KByte upto 2MByte for each slot can be arranged. The resulting base address must be added to the following values.

IP-Module A Memory Select	\$000000 - \$03FFFF	256KByte Range
IP-Module B Memory Select	\$040000 - \$07FFFF	256KByte Range
IP-Module C Memory Select	\$080000 - \$0BFFFF	256KByte Range
IP-Module D Memory Select	\$0C0000 - \$0FFFFF	256KByte Range
IP-Module A Memory Select	\$000000 - \$07FFFF	512KByte Range
IP-Module B Memory Select	\$080000 - \$0FFFFF	512KByte Range
IP-Module C Memory Select	\$100000 - \$17FFFF	512KByte Range
IP-Module D Memory Select	\$180000 - \$1FFFFF	512KByte Range
IP-Module A Memory Select	\$000000 - \$0FFFFF	1MByte Range
IP-Module B Memory Select	\$100000 - \$1FFFFF	1MByte Range
IP-Module C Memory Select	\$200000 - \$2FFFFF	1MByte Range
IP-Module D Memory Select	\$300000 - \$3FFFFF	1MByte Range
IP-Module A Memory Select	\$000000 - \$1FFFFF	2MByte Range
IP-Module B Memory Select	\$200000 - \$3FFFFF	2MByte Range
IP-Module C Memory Select	\$400000 - \$5FFFFF	2MByte Range
IP-Module D Memory Select	\$600000 - \$7FFFFF	2MByte Range

Note !

After a hardware reset the memory select area is disabled to avoid the loss of important address space. This feature might be advantageous, if IO-select working IP-modules are used.

6.2 Onboard IP-Slots A & B

The IP003 offers two slots to carry either two single high IP- Modules or one double high module. The 50 pin DSUB connector ST3 supplies module A with all necessary logic signals, while module B uses ST4. The opposite DSUB connectors ST5 and ST6 contain the I/O interface signals. They are located on an IPAxx adapter board, which allows for different I/O connection facillities. The standard IPA01 board connects the 50 lines of each module to two 50 pin wrap connectors for flat cable mounting. Any other cable connection can be realized by another IPAxx adapter board.
Each slot is equipped with a fused 5 volt and a non fused +/-12 volt supply. The soldered fuse is rated for 2AT and should only be replaced by the same kind and type. The component mounting hight underneath the IP module area is realized below 3mm (0.11inch) to allow for a good air flow between the carrier board and the I-Packs. The component free area contains a separated copper layer for enhanced noise protection. It can be inductive, capacitiv or resistiv connected to the logic ground layer of the IP003 or left floating. A 5.08mm (0.2inch) gap between the logic interface connector and the I/O interface connector allows for a proper galvanic isolation.
Each slot is supplied with ID-, I/O- and memory select lines. All signals concerning the DMA controlled cycles are not used and tied to a logical high by pullup resistors. The reserved pins of slot A are connected to the reserved pins of slot B.
The strobe lines of slot A & B, STRBA & STRBB can be accessed via the board control buffer, located at $x800 within the VMEbus Short I/O range. The value of the VMEbus data line D4 will cause the state of the STRBA line, data line D5, that of the STRBB line.
The BCR will accept byte sized write accesses on odd byte adress boundaries or word write accesses on even word boundaries, however, only the lower data byte must contain valid data. The upper byte of the BCR is read only, but a write access to the upper byte will cause no error.
The state of the slot A & B error lines, PERRA* & PERRB*, will be reflected within the upper byte of the BCR. If the slot A error line is in a low state, the VMEbus data line D12 will be low during read accesses of the BCR. The slot B error line can be checked on data line D13.
For more information about the BCR, please refer to 8. Description of the Board Control Register.

Pin assignment of the logical interface connectors ST3 and ST4

DSUB Connector Pin:		Signal Name:	
1	26	GND	GND
2	27	CLOCK	+5V/1A
3	28	RESET	R/W*
4	29	D0	ID-Sel*
5	30	D1	(DMAReq0*)
6	31	D2	MEM-Sel*
7	32	D3	(DMAReq1*)
8	33	D4	INT-Sel*
9	34	D5	(DMAck*)
10	35	D6	I/O-SEL*
11	36	D7	(reserved 0)
12	37	D8	A1
13	38	D9	(DMAEnd*)
14	39	D10	A2
15	40	D11	ERROR*
16	41	D12	A3
17	42	D13	IRQ0*
18	43	D14	A4
19	44	D15	IRQ1*
20	45	LDS*	A5
21	46	UDS*	STROBE*
22	47	-12V	A6
23	48	+12V	ACK*
24	49	+5V/1A	(reserved 1)
25	50	GND	GND

Signals within brackets are not used !
An '*' indicates a low active signal.

6.3 Piggyback IP-Slots C & D (IE 003)

The IP003 offers two further slots for two single high IP-Modules or one double high module by the use of the IE003 extension board. This piggyback fits onto the 64pin VG connector ST2, which contains all necessary control signals to support to more I-Packs. The IE003 performs the signal distribution to its two 50 pin DSUB connectors from the VG connector and it uses also an IPAxx adapter board, which allows different I/O connection facillities.
Each slot is equipped with a fused 5 volt and a non fused +/-12 volt supply. The soldered fuse is rate for 2AT and should only be replaced by the same kind and type. The component mounting height underneath IP module area is realized below 3mm (0.11inch) to allow a good air flow between the carrier board and the I-Packs. The component free area contains a separated copper layer for enhanced noise protection. It can be inductive, capacitive or resistive connected to the logic ground layer of the IP003 or left floating. A 5.08mm (0.2inch) gap between the logic interface connector and the I/O interface connector allows a proper galvanic isolation.
Each slot is supplied with ID-, I/O- and memory select lines. All signal concerning the DMA controlled cycles are not used and tied to a logical high by pullup resistors. The reserved pins of slot C are connected to the reserved pins of slot D.
The strobe lines of slot C & D, STRBC & STRBD can be accessed via the board control buffer, located at $x800 within the VMEbus Short I/O range. The value of the VMEbus data line D6 will cause the state of the STRBC line, data line D7, that of the STRBD line.
The state of the slot C & D error lines, PERRC* & PERRD*, will be reflected within the upper byte of the BCR. If the slot C error line is in a low state, the VMEbus data line D14 will be low during read accesses of the BCR. The slot D error line can be checked on data line D15.

The pin assignment of the piggyback extension VG connector ST2

Connector ST2A	Pin	Connector ST2B
Ground	1	Ground
D15	2	D14
D13	3	D12
D11	4	D10
D9	5	D8
D7	6	D6
D5	7	D4
D3	8	D2
D1	9	D0
Ground	10	Ground
A6	11	UDS*
A5	12	LDS*
A4	13	R/W*
A3	14	(DMA-Done*)
A2	15	RESET*
A1	16	CLOCK
+5V	17	+5V
Ground	18	Ground
+12V	19	-12V
not connected	20	not connected
ID-Sel-C*	21	MEM-Sel-C*
INT-Sel-C*	22	Error-C*
I/O-Sel-C*	23	Acknowledge-C*
Strobe-C	24	Interrupt1-C*
Interrupt0-C*	25	(DMA-Acknowledge-C*)
(reserved 2)	26	(reserved 3)
ID-Sel-D*	27	MEM-Sel-D*
INT-Sel-D*	28	Error-D*
I/O-Sel-D*	29	Acknowledge-D*
Strobe-D	30	Interrupt1-D*
Interrupt0-C*	31	(DMA-Acknowledge-C*)
Ground	32	Ground

Signals within brackets are not used !
An '*' indicates a low active signal.

7. Standard Access Address Programming

The memory select line of each of the four IP modules requires - according to the specification - 8MBytes addressing range. This would cause a single carrier board with two I-Packs to cover the whole standard VMEbus addressing range. Usually only a small part or no memory select at all, is used onboard most of the IP modules. Therefore the address decoding range of the memory select area can be programmed onboard the IP003 within two shift registers. The state of the VMEbus address lines from A18 to A23 is compared to the contents of the compare shift register and, if the according mask shift register bit is set to zero, they are used for decoding. The programming of the shift registers is performed in the following manner.

1.step:
Clear all registers, i.e. set all register bits to zero by a byte read access to the address location $001, or a word sized read access to the location $000. This function is automatically performed by a hardware reset. After a reset, the contents of both shift registers is set to zero and the VMEbus standard access area is disabled at all. The I/O- and ID-Select lines, which can be accessed within the VMEbus short I/O range, are not affected by the reset function.

2.step:
Shift in 8 data bits into the address compare shift register, located at $x000, by 8 byte write cycles on odd byte address boundaries, or by 8 word write cycles on even word boundaries via the VMEbus data line D0. The first bit is used to enable the memory select range, the second bit selects two or four memory module slots.The state of the third data bit, shifted in, will be compared with the VMEbus address line A23, the last with address line A18.

3.step:
Shift in 8 data bits into the address mask shift register, located at $x400, by 8 byte write cycles on odd byte address boundaries, or by 8 word write cycles on even word boundaries via the VMEbus data line D0. The first data bit, if set to high, enables the slot A only function, the second data bit is used to select the two or three clock cycle mode. The data bit, shifted in as a logical zero, will mask out the VMEbus address line A23, the last, address line A18.

The mask bits enable various slot sizes according to the following table.

Slot decoding size

4 slots enabled:	A23	A22	A21	A20	A19	A18	2 slots enabled:
4MByte, 4 slots	1	1	1	1	1	1	8MByte, 2 slots
2MByte, 4 slots	0	1	1	1	1	1	4MByte, 2 slots
1MByte, 4 slots	0	0	1	1	1	1	2MByte, 2 slots
512KByte, 4 slots	0	0	0	1	1	1	1MByte, 2 slots
256KByte, 4 slots	0	0	0	0	1	1	512KByte, 2 slots
256KByte, 2 slots	0	0	0	0	0	1	512KByte, 1 slot
256KByte, 1 slot	0	0	0	0	0	0	256KByte, 1 slot

Address compare shift register bit overview

Contents of bit:	7	6	5	4	3	2	1	0	
any state	x	x	x	x	x	x	x	x	
clear:	0	0	0	0	0	0	0	0	(contents after reset)
1.write	0	0	0	0	0	0	0	a	
2.write	0	0	0	0	0	0	a	b	
3.write	0	0	0	0	0	a	b	c	
4.write	0	0	0	0	a	b	c	d	
5.write	0	0	0	a	b	c	d	e	
6.write	0	0	a	b	c	d	e	f	
7.write	0	a	b	c	d	e	f	h	
8.write	a	b	c	d	e	f	g	h	
	|	|	|	|	|	|	|	|	
is compared with	MSEN	MSWC	A23	A22	A21	A20	A19	A18	

MSEN: Memory select enable, active high
MSWC: Module switch, low 0 = 2 modules, high = 4 modules

Address mask shift register bit overview

Contents of bit:	7	6	5	4	3	2	1	0	
any state	x	x	x	x	x	x	x	x	
clear:	0	0	0	0	0	0	0	0	(contents after reset)
1.write	0	0	0	0	0	0	0	a	
2.write	0	0	0	0	0	0	a	b	
3.write	0	0	0	0	0	a	b	c	
4.write	0	0	0	0	a	b	c	d	
5.write	0	0	0	a	b	c	d	e	
6.write	0	0	a	b	c	d	e	f	
7.write	0	a	b	c	d	e	f	h	
8.write	a	b	c	d	e	f	g	h	
	|	|	|	|	|	|	|	|	
is compared with	SLTA	CMDE	A23	A22	A21	A20	A19	A18	

SLTA: Slot A only enable, high enables only slot A within the memory range
CMDE: Clock mode enable, high selects 2 cycle clock mode, low selects 3 cycle mode

The final state of both shift registers is not locked and any further write command will shift the register contents by one additional step. The contents of both shift registers is write only and cannot be read back.

7.1 Board specific parameters

The VMEbus 'LDS' data strobe line, controlling the VMEbus data lines D0 to D7 activates the IP slot byte select line for the IP slot data lines D0 to D7. The VMEbus 'UDS' data strobe line controlls the remaining data lines D8 to D15.

As a standard access timing, the 3 clock cycle sequence is implemented within the PLSI. The 2 clock cycle sequence can be activated by software, but the user should verify, that the used IP modules are able to work in this fast termination mode.

After a reset, the standard 3 cycle mode is enabled. The 2 cycle mode can be set by programming bit 6 in the address mask shift register to high.

7.2 The 3 clock access timing

	clock speed	8 MHz/125ns	
1.	select phase	activated signals	select line address lines A1 - A22 byte select lines read/write line data on write cycles
2.	hold phase	deactivated signals check and wait for	address lines A7 - A22 acknowledge line active
3.	terminate phase	deactivated signals	select line address lines A1 - A6 byte select lines read/write line data on write cycles

7.3 The 2 clock access timing

	clock speed	8 MHz/125ns	
1.	select phase	activated signals	select line address lines A1 - A22 byte select lines read/write line data on write cycles
2.	terminate phase	deactivated signals	select line address lines A1 - A6 byte select lines read/write line data on write cycles

7.4 Example for base address setting in assembler

```
*******************************************************************
*      IP003 VMEbus Standard Access Address Selection            *
*******************************************************************
*
IBASE     EQU      $3000      ; code switch position 3
*
IPSRC     EQU      $001       ; clear shift register (rd)
IPCRG     EQU      $001       ; address compare register (wr)
IPMRG     EQU      $401       ; address mask register (wr)
IPBCR     EQU      $800       ; board control register (r/w)
*
*      clear both shift registers
*
       MOVE.B    #$F8,IBASE+IPBCR  ; set no ints & level 0
       MOVE.B    IBASE+IPSRC,D0    ; clear shift register
*
*      set for 1 memory select enable, 0 = memory select disable
*
       MOVE.B    #$1,IBASE+IPCRG   ; enable memory select
*
*      set 1 for 4 IP modules, 0 for 2 IP modules
*
       MOVE.B    #$0,IBASE+IPCRG   ; set for 2 IP modules
*
*      set std.access address to $600000
*
       MOVE.B    #$0,IBASE+IPCRG   ; compare to A23
       MOVE.B    #$1,IBASE+IPCRG   ; compare to A22
       MOVE.B    #$1,IBASE+IPCRG   ; compare to A21
       MOVE.B    #$0,IBASE+IPCRG   ; compare to A20
       MOVE.B    #$0,IBASE+IPCRG   ; compare to A19
       MOVE.B    #$0,IBASE+IPCRG   ; compare to A18
*
*      set 1 for slot A only mode, 0 for normal mode
*
       MOVE.B    #$0,IBASE+IPMRG   ; set normal mode
*
*      set 1 for 2 clock cycle mode, 0 for 3 clock cycle mode
*
       MOVE.B    #$0,IBASE+IPMRG   ; set 3 clock cycle mode
*
*      mask address lines for 2 x 512KByte slots
*
       MOVE.B    #$0, IBASE+IPMRG  ; do not mask A23
       MOVE.B    #$0, IBASE+IPMRG  ; do not mask A22
       MOVE.B    #$0, IBASE+IPMRG  ; do not mask A21
       MOVE.B    #$0, IBASE+IPMRG  ; do not mask A20
       MOVE.B    #$1, IBASE+IPMRG  ; mask A19
       MOVE.B    #$1, IBASE+IPMRG  ; mask A18
*
*      slot A: $600000 - $67FFFF
*      slot B: $680000 - $6FFFFF
*      slot C: no select
*      slot D: no select
*
*
       END
/*************************************************************************/
```


7.5 Example for base address setting in "C"

```
/*********************************************************************/
/*   MODULE:  ip003.c                                               */
/*   DATE:    99/04/30                                              */
/*   PURPOSE: This application enables memory select on IP003       */
/*                                                                  */
/*------------------------------------------------------------------*/
/*                                                                  */
/* Edition History:                                                 */
/*                                                                  */
/* Ed   Data         Comment                                     by */
/* ---- --------  -----------------------------------------------  -- */
/* 01   99/04/30  created                                        wa */
/*********************************************************************/
_asm("_sysedit:     equ  1");

#include <const.h>
#include <stdio.h>
#include <errno.h>
#include <modes.h>
#include <process.h>
#include <sgstat.h>
#include <sg_codes.h>
#include <regs.h>
#include <types.h>
#include <cache.h>


#define    IPBASE        0xFF00F000

#define    MASK_512K     0x000C0000

/*---------------------------------------------------------------------*/
/* some IP003 Control and Status Registers                             */
/*---------------------------------------------------------------------*/
#define   IPSRC              *((volatile u_char*)(IPBASE + 0x01))
#define   IPCRG              *((volatile u_char*)(IPBASE + 0x01))
#define   IPMRG              *((volatile u_char*)(IPBASE + 0x401))
#define   IPBCR              *((volatile u_short*)(IPBASE + 0x800))

void usage(void)
{
     fprintf(stderr,"Syntax: ip003 <Baseaddress> <level>\n");
     fprintf(stderr,"Function: Set Memory Base and IRQ Vector on IP003\n");
     exit(1);
}
```

```
main(int argc, char ** argv, char ** envp)
{
     int i;
     u_int32 base;
     u_int32 mask;

     int level;
     u_char sink;

     process_id proc_id;
     u_int16 priority;
     u_int16 age;
     u_int32 schedule;
     u_int16 group;
     u_int16 user;

     error_code result;

     if (argc != 3)
          usage();

     sscanf(argv[1], "%x",&base);
     sscanf(argv[2], "%x",&level);


     base &= 0x00ffffff;           /* 24 bit address only */

     if ((level < 0) || (level > 7))
     {
          printf("illegal IRQ Level ! \n");
          _os_exit(0);
     }

     _os_id(&proc_id, &priority, &age, &schedule, &group, &user);

     if (errno =_os_permit ((void*)IPBASE , 0x1000, _READ|_WRITE, proc_id))
     {
          printf("no access permission to IP003\n");
          _os_exit(errno);
     }

     _os_cache(C_DISDATA|C_FLDATA, (void*)IPBASE, 0x1000);
```



```
/*----------------------------------------------------------------------*/
/* Set IP003 FIFO.                                                      */
/*----------------------------------------------------------------------*/

     IPBCR = level | 0x00F8;           /* set irq level */

     sink = IPSRC;                     /* clear shift register */

     IPCRG = 0x01;                     /* enable memory select */
     IPCRG = 0x00;                     /* 2 modules */

     base = base <<8;

     /* write base address to FIFO */

     for (i=0; i<6; i++)
     {
          if ((base & 0x80000000) == 0)     /* A23..A18 to FIFO */
               IPCRG = 0x00;
          else
               IPCRG = 0x01;

          base  = base << 1;
     }

     IPMRG = 0x00;                     /* normal mode */

     IPMRG = 0x01;                     /* 2 clock cycle mode */

     mask = MASK_512K << 8;

     /* write size mask to FIFO */

     for (i=0; i<6; i++)
     {
          if ((mask & 0x80000000) == 0)     /* A23..A18 to FIFO */
               IPMRG = 0x00;
          else
               IPMRG = 0x01;

          mask  = mask << 1;
     }


     _os_cache(C_ENDATA, (void*)IPBASE, 0x1000);

}
```

8. The Board Control Register

The IP003 contains a 16 bit wide control register for board maintenance. It is partly read/write and read only according to the following bit map. The access address is located within the VMEbus short I/O range with an address offset of $x800 to the selectable board base address. The BCR accepts byte sized write accesses on odd byte adress boundaries or word write accesses on even word boundaries, however only the lower data byte must contain valid data. The upper byte of the BCR is read only, but a write access to the upper byte will cause no error.
The read/write part contains the interrupt level and enable bits, and the four IP-Module strobe lines. The read only segment uses only four bits out of eight for the IP-Module error lines. The remaining bits are tied to a logical high level.

The Board Control Register Bit Map:

The Read Only Part:

D15	D14	D13	D12	D11	D10	D9	D8
|	|	|	|				
Error D	Error C	Error B	Error A		not used		

The Read/Write Part:

D7	D6	D5	D4	D3	D2	D1	D0
|	|	|	|	|	MSB		LSB
Strobe D	Strobe C	Strobe B	Strobe A	Interrupt Enable		Interrupter Level	

Error A:	IP-Modul A error line, low active.
Error B:	IP-Modul B error line, low active.
Error C:	IP-Modul C error line, low active.
Error D:	IP-Modul D error line, low active.
not used:	reflects always high level.
Strobe A:	IP-Module A strobe line, any function.
Strobe B:	IP-Module B strobe line, any function.
Strobe C:	IP-Module C strobe line, any function.
Strobe D:	IP-Module D strobe line, any function.
Interrupt Enable:	VMEbus interrupter enable, low active.
Interrupter Level:	VMEbus interrupter level, binary, high active.

9. The VMEbus Interface

The bus interface of the IP003 is designed according to the VMEbus specification ANSI/IEEE STD1014-1987, IEC 821 & 297. The VMEbus connector ST1 contains on the row A, B and C all standard VMEbus lines, necessary for A16/A23, D8/D16 slave boards. All unused daisy chain lines are linked through, i.e. no external bypass links are necessary. The address modifier signals AM0 to AM5 are a part of the VMEbus specifications and serve to differentiate between certain address areas. With the exception of the AM2 line, all others are used for the onboard decoding logic. The IP003 accepts accesses within the VMEbus short I/O range and the VMEbus standard access area.

The following AM-Codes are accepted by the IP003:

AM5	AM4	AM3	AM2	AM1	AM0	Access for	
H	H	H	H	L	H	Standard Supervisory Data	(3D)
H	H	H	L	L	H	Standard User Data	(39)
H	L	H	H	L	H	Short I/O Supervisory Data	(2D)
H	L	H	L	L	H	Short I/O User Data	(29)

L = logical low H = logical high

9.1 The VMEbus Interrupter

The IP003 is equipped with a programmable 7 level VMEbus interrupter. The desired level can be loaded into the board control register. The interrupt vector must be supplied by the according IP-Module. The eight interrupt sources of the four posssible IP-Modules are preprocessed by an eight state round robin interrupt handler. Each IP-Slot contains the two interrupt sources 0 & 1. The slots are marked with A, B, C and D. The round robin scheduler works according to following state scheme.

... - A0 - B0 - C0 - D0 - A1 - B1 - C1 - D1 - A0 - B0 - ...

If any other interrupt processing sequence is desired, the contents of the INT-PLSI must be modified.

The board control register, located at $x800, contains four control bits for the VMEbus interrupter. Three bits are used as the binary coded, high active, VMEbus interrupt level, one bit enables or disables the interrupt function at all. The BCR data lines D0 to D2 represent the interrupter level, the data bit D3 enables the interrupter, if set to low. After a hardware reset, the contents of the BCR is not defined, and may have any state.

Bit Map of the VMEbus Interrupter Level:

Data Bit:	D0	D1	D2	D3
disable:	x	x	x	1
disable:	0	0	0	x
Level 1:	1	0	0	0
Level 2:	0	1	0	0
Level 3:	1	1	0	0
Level 4:	0	0	1	0
Level 5:	1	0	1	0
Level 6:	0	1	1	0
Level 7:	1	1	1	0

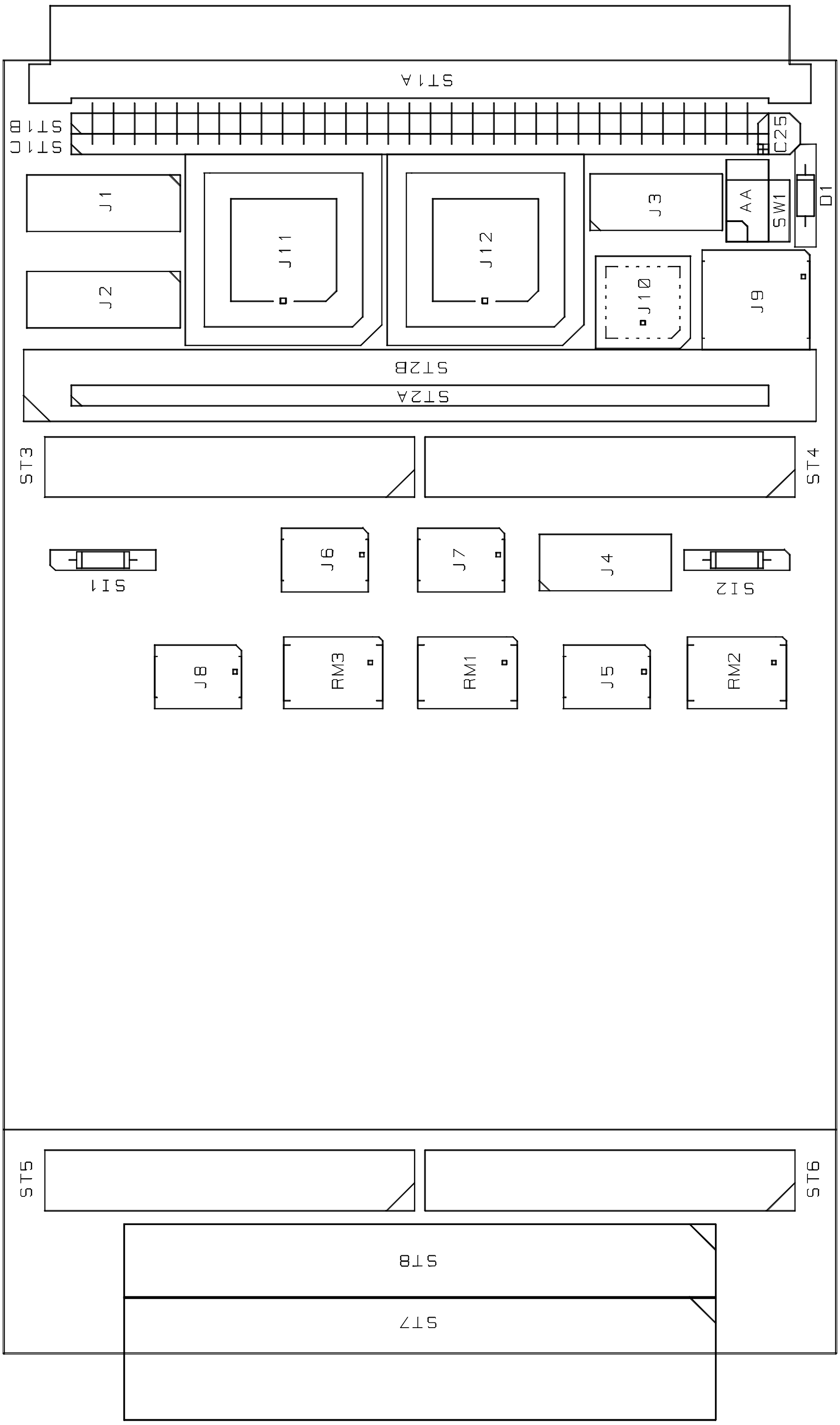
(x = don't care)

If the data bit D3 of the BCR is set to one or the data bits D0 to D3 are set to zero, no interrupt will be generated at all and any interrupt request from the IP-Modules will be ignored. The lower part of the board control register from D0 to D7 can be read back for verification, the upper part from D8 to D15 is read only.

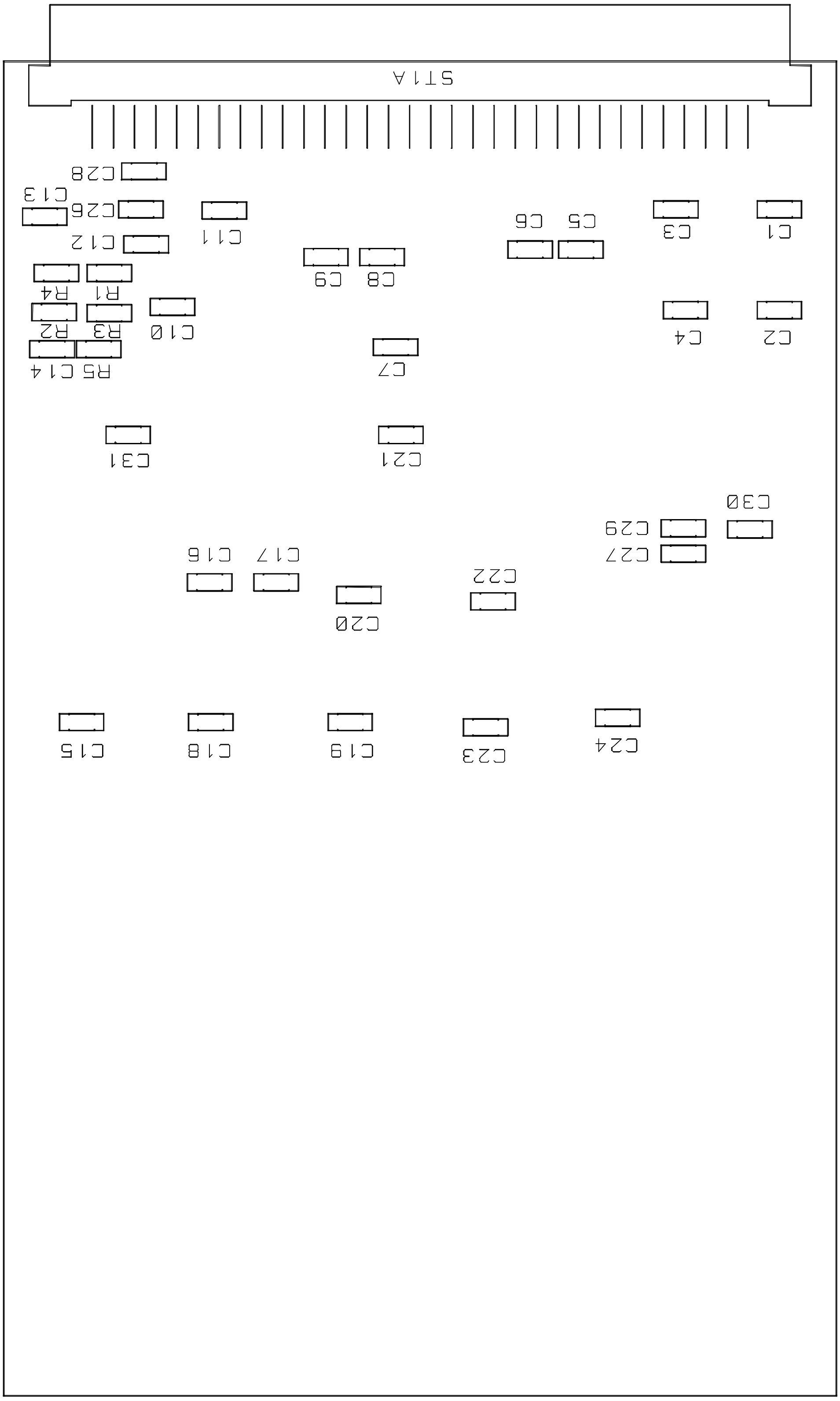
9.2 Pin Assignment of the VMEbus Connector ST1

Pin	Row A	Row B	Row C
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	(BG0IN*)	D11
5	D04	(BG0OUT*)	D12
6	D05	(BG1IN*)	D13
7	D06	(BG1OUT*)	D14
8	D07	(BG2IN*)	D15
9	GND	(BG2OUT*)	GND
10	SYSCLK	(BG3IN*)	(SYSFAIL*)
11	GND	(BG3OUT*)	BERR*
12	UDS*	(BR0*)	SYSRESET*
13	LDS*	(BR1*)	LWORD*
14	R/W*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	(AM2)	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	—	A17
22	IACKOUT*	—	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	(5VSTB)	+12V
32	+5V	+5V	+5V

Appendix A: IP 003 Layout Component Side



Appendix B: IP 003 Layout Solder Side

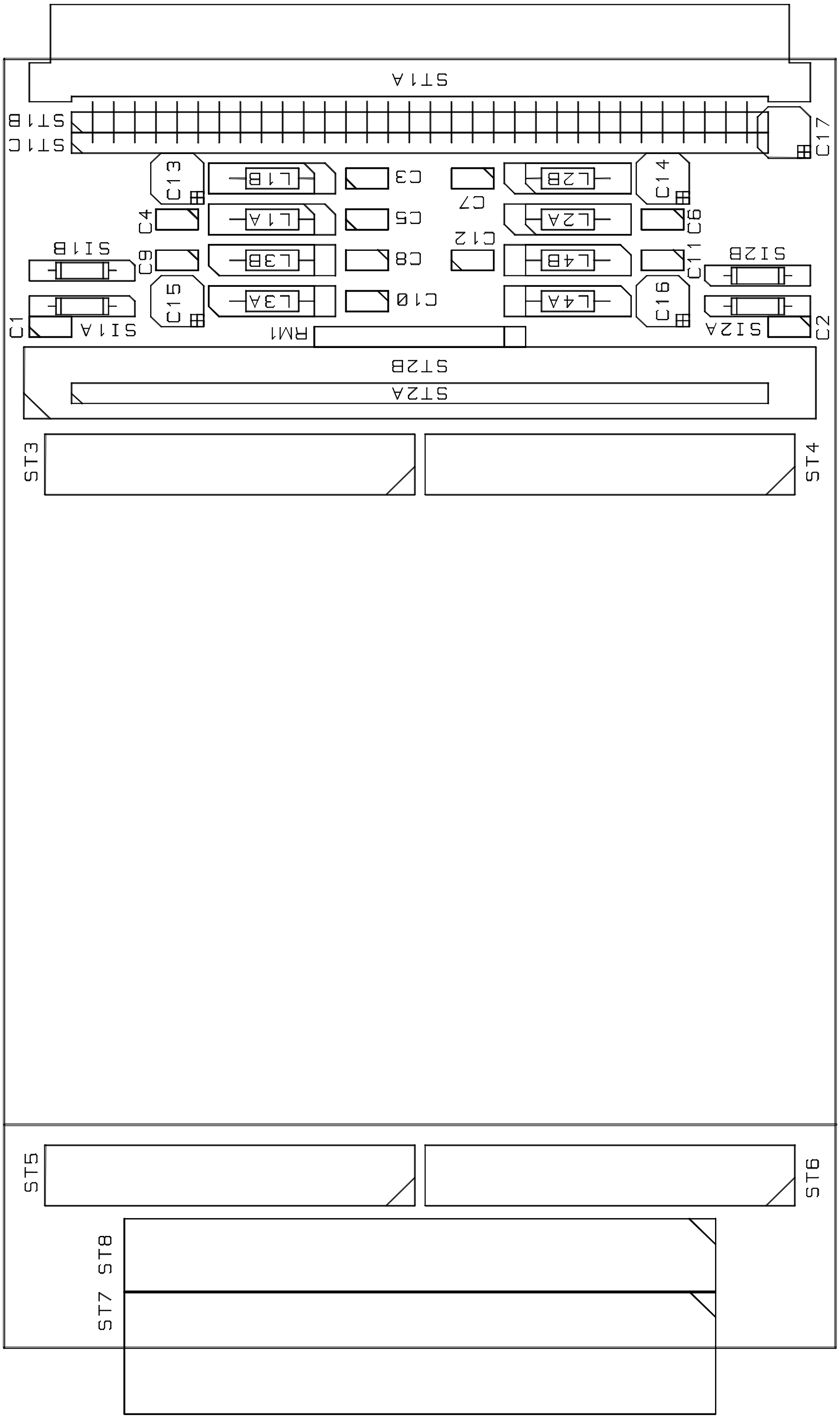


Appendix C: Edition History

Edition	Date	Description of Changes
1	April 1994	Initial issue for IP003
2	December 1995	Address compare- and mask shift register description changed on pages 13 and 14 corresponding to new PLSI No. 2460203. 2 and 3 cycle description added on page 15. Programming example adopted to new register layout on page 16.
3	April 1997	Minor changes on page 2, 4, 6, 9, 11, 18. Appendix E: IE003 Layout Component Side and Appendix F: IE003 Schematics added. 2nd edition changed to 3rd edition.
4	August 1997	Minor changes on page 16
5	October 1999	Assembler example program corrected and "C" program added page 16ff

Appendix D: IP 003 Schematics

Appendix E: IE 003 Layout Component side



Appendix F: IE 003 Schematics