

# **Microsys**

**User's Manual**

**ET003 Rev. 1**

**3<sup>rd</sup> edition**

# Declaration of Conformity

We, Manufacturer  
MicroSys Electronics GmbH  
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Germany

declare that the product

**ET003**

is in conformity with:

**EN 50081-1 Generic emission standard**  
**EN 50082-1 Generic immunity standard**

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above-mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date: 02. 06. 1999

Signature:

Position: General Manager

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## Edition

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# 1. Introduction

## 1.1 Board Overview:

LANCE Memory:	256Kb, complete RAM area is real dual ported for the LANCE at no waitstate and the VMEbus.
LANCE Controller:	AMD AM-7990, with on chip DMA
Transceiver:	Intel 82503 with AUI and TP support
Node-ID:	32Bit unique board specific node identification code
Interrupter:	7 level & vector programmable VMEbus interrupter
Front panel:	6 board state leds 15 pin DSUB connector for Ethernet AUI RJ45 connector for 10bAse-t

## 1.2 Specifications

– Environmental Requirements:

Operating Temperature	0 degrees C to + 70 ° C
Relative Humidity	0 to 95% (non-condensing)
Storage Temperature	-15 °C to +85 °C
Power Requirements	5V, 350mA typical 12V for external AUI support

– Board Dimensions:

Single Euro Format:	Length: 160mm (6.3 inches) Width: 100mm (3.9 inches)
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**003** can be supplied with single 5 volts, if the optional connected MAU does not use the supply.

## 1.3 Related Documentation

**The following manuals are applicable to the ET 003:**

- AM7990 Local Area Network Controller for Ethernet (LANCE) User's Manual
- Intel 82503 User's Manual

## 2. Delivery

### 2.1 Items shipped with this unit

- User's Manual ET 003 Hardware
- MicroSys shipping carton



**ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT**

### 2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys Shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moist free, dust free environment. The storage temperatures and humidity specifications are shown in chapter 1

## 3. Installation

### 3.1 Items required for ET 003 installation

For installation of the ET 003, the following items are required.

- VMEbus System with CPU
- Adequate rated power supply

### 3.2 Points to be observed with unit

Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +5V ( + 5 %, - 2,5 % ),  
+12V ( + 5 %, - 2,5 % ) is only necessary for AUI interface.
- Be sure voltage is of correct polarity
- Unit should only be inserted into, and removed from card cage when power is off.
- The card cage should be well ventilated. The operating temperature should never exceed  
it's specified range.
- Check default jumper setting.



**GUARANTEE IS VOID IF UNIT IS OPERATED  
OUT OF ITS SPECIFICATIONS!**

## 4. VMEbus Address map ET 003:

Type	Range	End	Comment
AM7990 LANCE	X0 0000	X0 0003	16 Bit, word access only
Node ID	X0 0800	X0 080A	8 Bit, read only, D8-D15
Vector Register	X0 0801	X0 0801	8 Bit, read/write, D0-D7
Interrupt Level Bit 1	X0 0803	X0 0803	read/write - set/clear
Interrupt Level Bit 2	X0 0805	X0 0805	read/write - set/clear
Interrupt Level Bit 3	X0 0807	X0 0807	read/write - set/clear
SRAM Bank	X8 0000	XB FFFF	16 Bit, 256KB LANCE shared

**X:** VMEbus Standard Access Range Base Address selected via SW1



**Note!** Due to onboard DMA transfers that may delay VMEbus accesses, the timeout counter of your master CPU must be set to a minimum of 16µs to avoid Buserrors.

## 5. Dual Ported SRAM:

Two standard SRAMs with 128K organized represent the dual ported ram area for the network controller and the VMEbus. The LANCE is able to work within this ram area with zero waitstates. During the LANCE arbitration from bus slave to bus master, an additional waitstate may be inserted. The LANCE bus arbitration is only performed to allow slave accesses on the network controller.

The address decoding is made in 1MByte steps. The image of the RAM area appears several times within the decoded range.

### 5.1 VMEbus base address selection switch SW1:

Code Switch SW1	Address Range:
Position 0	\$000000 - \$0FFFFFFF
Position 1	\$100000 - \$1FFFFFFF
Position 2	\$200000 - \$2FFFFFFF
Position 3	\$300000 - \$3FFFFFFF
Position 4	\$400000 - \$4FFFFFFF
Position 5	\$500000 - \$5FFFFFFF
Position 6	\$600000 - \$6FFFFFFF
Position 7	\$700000 - \$7FFFFFFF
Position 8	\$800000 - \$8FFFFFFF
Position 9	\$900000 - \$9FFFFFFF
Position A	\$A00000 - \$AFFFFFFF
Position B	\$B00000 - \$BFFFFFFF
Position C	\$C00000 - \$CFFFFFFF
Position D	\$D00000 - \$DFFFFFFF
Position E	\$E00000 - \$EFFFFFFF
Position F	\$F00000 - \$FFFFFFF

**On shared ram access the VME-AM-Codes are decoded as follows:**

AM5	AM4	AM3	AM2	AM1	AM0	Access for
H	H	H	H	L	H	Standard Superv. Data (3D)
H	H	H	L	L	H	Standard User Data (39)

L = logical low

H = logical high

## 6. Local Area Network Controller:

The LANCE is able to communicate with its master by direct access, the dual port ram or via interrupts. For direct access only word transfers are allowed from the VMEbus. The direct communication with the LANCE chip is performed in the address range from \$X00000 to \$X007FE. The register address selection is done by address line A1, which is connected to the ADR input line of the Am7990. The data port register is selected if the ADR line is set to low, i.e. even longword boundaries, while the address port register is active on odd longword address boundaries. The internal byte-swapping feature of the network controller Am7990 must be set to:

BSWP = 1  
and BCON = 1,

To ensure proper data transfer between the LANCE and the dual port ram. The BM0 and BM1 byte mask feature of the LANCE is not used on the ET003. Any transfer to or from the dual port ram by the LANCE does not disturb an access by the VMEbus nor does the LANCE request the VMEbus.

The Am7990 does not support a vector controlled interrupt scheme, so the vector must be loaded into the interrupt vector register located at \$X00801. The vector register is read/write and can be read back for verification.

A reset will cause the LANCE to cease operation, clear its internal logic and enter the idle state. The contents of the dual port ram are not affected by a reset.



**For detailed chip information see  
Technical Description Am7990**

## 6.1 Node Identification Code:

There is a 48 bits long and board unique Node-ID code (MAC address) available on the ET003. The code can be accessed with read cycles on even byte address boundaries within the address range from \$X00800 to \$X0080A.

### Address map of the Node-ID code, present on data lines D8 to D15

X0 0800	1. Byte of Node-ID
X0 0802	2. Byte of Node-ID
X0 0804	3. Byte of Node-ID
X0 0806	4. Byte of Node-ID
X0 0808	5. Byte of Node-ID
X0 080A	6. Byte of Node-ID

## 6.2 Serial Transceiver:

The transceiver 82503 adapts an AUI and 10BASE-T interface to the single ended lines of the Am7990. All communication lines are isolated by a pulse transformer to protect the board and system from an external fault condition at the AUI connection cable or at the 10BASE-T interface. The 82503 automatically selects the connected port and also supports automatic polarity correction on the 10BASE-T interface.

The network status is displayed by the front panel leds Rx, Tx, CL, LI and PO.

The 15 pins DSUB front panel connector allows an external transceiver to be connected.

### Pin assignment of the front panel connector P2:

Pin:	1	_____	Ground
Pin:	2	_____	Collision+
Pin:	3	_____	Transmit+
Pin:	4	_____	Ground
Pin:	5	_____	Receive+
Pin:	6	_____	Ground
Pin:	7	_____	not connected
Pin:	8	_____	Ground
Pin:	9	_____	Collision-
Pin:	10	_____	Transmit-
Pin:	11	_____	Ground
Pin:	12	_____	Receive-
Pin:	13	_____	+12Volts
Pin:	14	_____	Ground
Pin:	15	_____	not connected



**Note!** The +12V must be supplied via VMEbus Pin 31c.

## 7. VME-Interrupter:

The ET003 supports interrupt generation on all 7 VMEbus levels. The desired interrupt level can either be set by the jumper field DA or, if all jumpers of DA are removed, by the three interrupt level registers. The binary coded level bits can be set (1) or cleared (0) by byte sized read or write commands to the address locations \$xx0803 for IL1, \$xx0805 for IL2 and \$xx0807 for IL3. The three level bits work as open collector outputs, i.e. any inserted link within jumper field DA will not cause any damage, but disable the level programming feature and release all outputs to high. The three level bits are set to high by a VMEbus reset.

The VMEbus interrupt vector is stored in the interrupter vector register. This 8 bit wide read/write register is located at the address \$X0 0801 and can be read back for verification. Byte or word sized write accesses are allowed, but only the data byte from D0 to D7 must contain valid data. The vector register is not cleared by a VMEbus reset and may have any contents after power up.

### Bit map of the VMEbus interrupter vector register:

<b>Data Bit:</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>
<b>Function:</b>	<b>MSB</b>	<b>Interrupter Vector</b>						<b>LSB</b>

### Hardware Jumper setting for VME interrupt request level:

<b>Jumper DA</b>	<b>1-2</b>	<b>3-4</b>	<b>5-6</b>
disable	X	X	X
Level 1	—	X	X
Level 2	X	—	X
<b>Level 3</b>	—	—	<b>X</b>
Level 4	X	X	—
Level 5	—	X	—
Level 6	X	—	—
Level 7	—	—	—

**X = link is installed      — = link is not installed**

**Level 3 is factory setting**

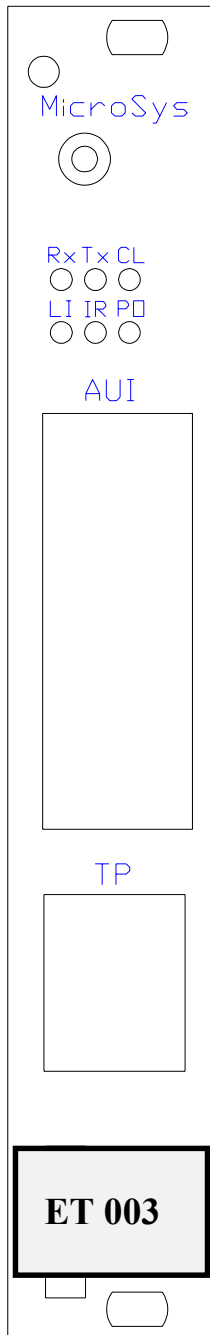
**Software programming for VME interrupt request level:**

Level 1	read \$xx0803	write \$xx0805	write \$xx0807
Level 2	write \$xx0803	read \$xx0805	write \$xx0807
Level 3	read \$xx0803	read \$xx0805	write \$xx0807
Level 4	write \$xx0803	write \$xx0805	read \$xx0807
Level 5	read \$xx0803	write \$xx0805	read \$xx0807
Level 6	write \$xx0803	read \$xx0805	read \$xx0807
Level 7	read \$xx0803	read \$xx0805	read \$xx0807



**Note! All links of Jumper DA must be removed to use software programming!**

## 8. Front Panel Description



**Rx = Receive** (green)  
**Tx = Transmit** (yellow)  
**CL = Collision** (red)

**LI= Link Integrity** (green)  
**IR = Interrupt** (yellow)  
**PO = Polarity** (red)

**15 Pin DSUB female Connector**

**Media Attachment Unit Port**

**RJ45 Connector**

**Ejector key**

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## 8.1 Front Panel LEDs:

**Rx LED:** This led indicates that data is received.

**Tx LED:** This led indicates that data is transmitted.

**CL LED:** This led indicates that a collision has occurred on the network cable.  
It will be illuminated only while the fault condition is active.

**LI LED:** This led shows the user, that the link on the 10BASE-T interface (RJ45)  
is correct

**IR LED:** This led indicates that a VMEbus IRQ is pending.

**PO LED:** This led is switched on when the polarity on the 10BASE-T connection is wrong.

## 8.2 Front Panel Connectors:

**RJ45:** This connector is used to attach 10BASE-T network hubs or switches.

Pin 1	Tx+
Pin 2	Tx-
Pin 3	Rx+
Pin 4	not connected
Pin 5	not connected
Pin 6	Rx-
Pin 7	not connected
Pin 8	not connected

**DSUB:** This 15 pin DSUB female connector contains the differential AUI lines, several board ground lines and the +12 volt line to support an external cheapernet or ethernet media attachment unit.

### Pin assignment of the AUI connector:

Pin 1	Board Ground
Pin 2	Collision+
Pin 3	Transmit+
Pin 4	Board Ground
Pin 5	Receive+
Pin 6	Board Ground
Pin 7	not connected
Pin 8	Board Ground
Pin 9	Collision-
Pin 10	Transmit-
Pin 11	Board Ground-
Pin 12	Receive-
Pin 13	+12Volts
Pin 14	Board Ground
Pin 15	not connected

## 9. VME-Bus Interface:

The VMEbus interface supports all VMEbus lines according to the VMEbus specifications ANSI / IEEE STD1014. The address bus is 24 bits, the data bus is 16 bits wide. The VMEbus connector P1 contains on the rows A, B, C all standard VMEbus lines. All VMEbus daisy-chain lines, which are not used onboard, are linked through.

The address modifier codes from AM0 to AM5 are a part of the VMEbus specifications and serve to differentiate between particular memory areas.

**The following AM codes are accepted by ET003:**

AM5	AM4	AM3	AM2	AM1	AM0	Access for
H	H	H	H	L	H	Standard Superv. Data (3D)
H	H	H	L	L	H	Standard User Data (39)
L = logical low			H = logical high			

## 9.1 Pin Assignment of VMEbus Connector P1:

Pin	Row A	Row B	Row C
1	D00	—	D08
2	D01	—	D09
3	D02	—	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	—	SYSRESET*
13	DS0*	—	LWORD*
14	WRITE*	—	AM5
15	GND	—	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	—	A17
22	IACKOUT*	—	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	—	—	+12V
32	+5V	+5V	+5V

## 10. Summary of Jumpers & Switches

Size	Jumper	Position	Function
3x2	DA	1-2	VMEbus Interrupter Level Bit 1
	DA	3-4	VMEbus Interrupter Level Bit 2
	DA	* 5-6	VMEbus Interrupter Level Bit 4

\* Means factory setting

**VME Interrupt Level 3 is default setting**

Code Switch SW1	Address Range:
Position 0	\$000000 - \$0FFFFFFF
Position 1	\$100000 - \$1FFFFFFF
Position 2	\$200000 - \$2FFFFFFF
Position 3	\$300000 - \$3FFFFFFF
Position 4	\$400000 - \$4FFFFFFF
Position 5	\$500000 - \$5FFFFFFF
Position 6	\$600000 - \$6FFFFFFF
Position 7	\$700000 - \$7FFFFFFF
<b>Position 8</b>	<b>\$800000 - \$8FFFFFFF</b>
Position 9	\$900000 - \$9FFFFFFF
Position A	\$A00000 - \$AFFFFFFF
Position B	\$B00000 - \$BFFFFFFF
Position C	\$C00000 - \$CFFFFFFF
Position D	\$D00000 - \$DFFFFFFF
Position E	\$E00000 - \$EFFFFFFF
Position F	\$F00000 - \$FFFFFFF

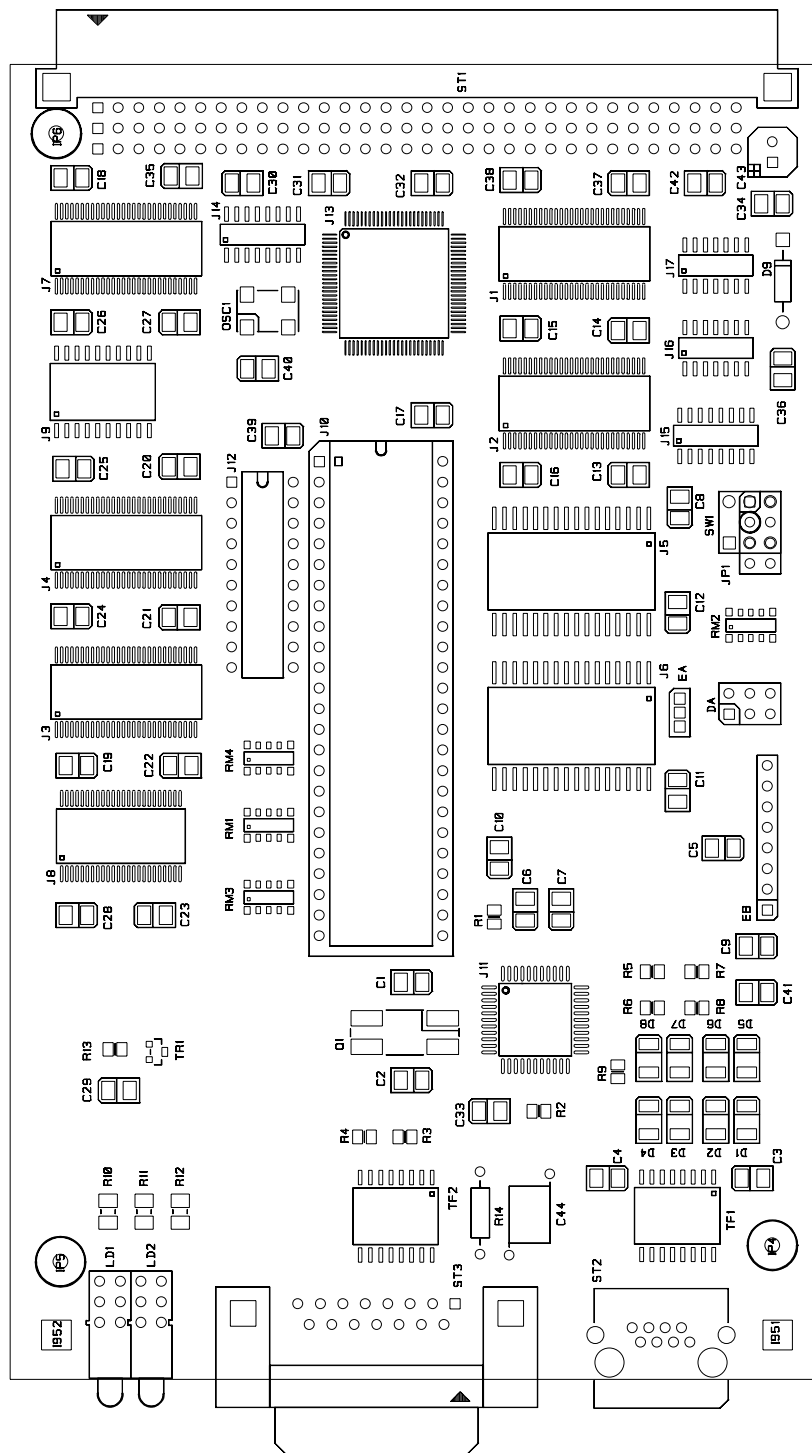
**Position 8 is default setting**



**Note! Boards with ispLSI version 2720102 allow even positions only. All odd positions lead to a Bus Error.**

## Appendices

# Appendix A: Layout Component Side



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## Appendix B: Schematics (in printed versions only)