MicroSys

User's Manual

CRX01 Rev. 2

preliminary

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
D-82054 Sauerlach
Germany

declare that the product

CRX01

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

Edition

	Date:	Ident-Nr.:	Released:
Manual	04.07.2006	EW309MA-02AA	
Schematics	12.06.2006	EW309SL-02AA	

MicroSys GmbH,
Mühlweg 1,
82054 Sauerlach,
Germany.

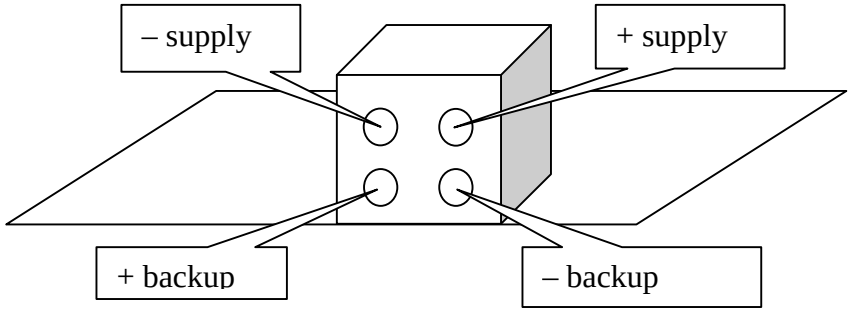
(ISDN)
Hotline (08104) 801-130,
Phone (08104) 801-0,
Fax (08104) 801-110.

Internet: http://www.MicroSys.de

Power Supply:

The CRX01 carrier must be supplied with DC power in the range from 12 to 24V either via connector PWRA or connector PWRB. The average power consumption of the CRX01 carrier without any mounted module is below 2 watts. The power supply of the CRX01 is reverse polarity protected and fused by a resetable 1.1A fuse. The backup input is protected against over voltage and wrong polarity, but the normal operating backup voltage should not exceed 3.6 volts.

PWRA / PWRB Connector Front view:



Attention! The pins "– backup" (pin 1) and "– supply" (pin 4) are internally connected!

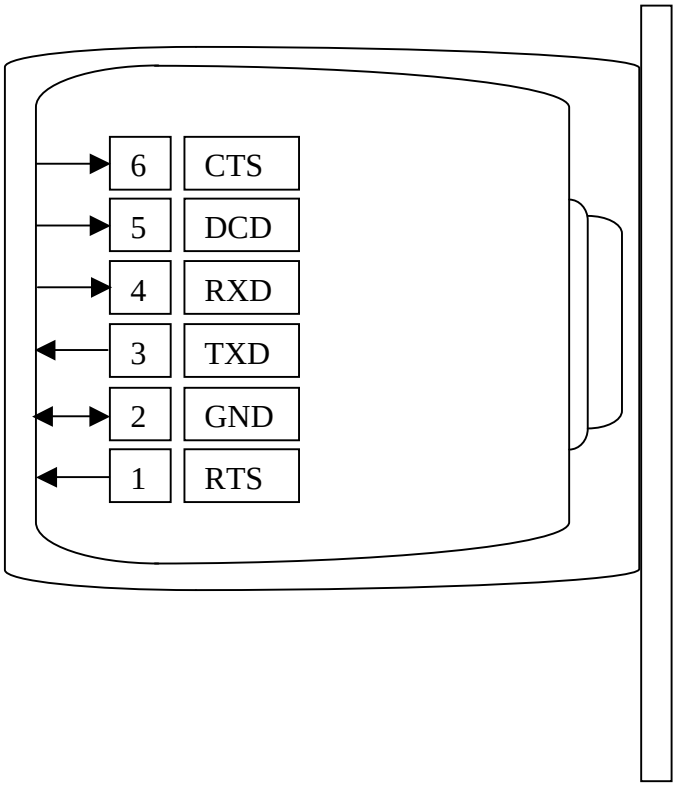
PWRA / PWRB Connector Pin out:

Pin:	PWRA	PWRB	Rating
1	GND	GND	
2	+Vbackup	+Vbackup	max.3.6VDC
3	+Vsupply	+Vsupply	12-24VDC
4	GND	GND	

The Serial Interface:

There are two RS232 serial interfaces onboard the CRX01, which are connected to the UART signals of module connector ST2-d. Depending on the used MPX module, only one or both channels with more or less handshake lines are supported. The interface is able to handle transfer rates up to 250kbps.

RJ11 Connector Front view



SIOA / SIOB Interconnection:

RJ11-SIOA			ST2	
Pin:	**RS232**		**Signal**	**Pin:**
1	RTS-1		URTS1/PSC1-2	d38
2	GND		---	---
3	TXD-1		UTXD1/PSC1-0	d34
4	RXD-1		URXD1/PSC1-1	d36
5	DCD-1		UDCD/PSC1-4	d42
6	CTS-1		UCTS1/PSC1-3	d40

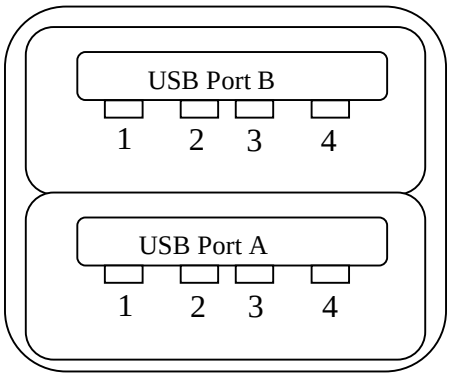
RJ11-SIOB			ST2	
Pin:	**RS232**		**Signal**	**Pin:**
1	RTS-2		URTS2/PSC2-2	d48
2	GND		---	---
3	TXD-2		UTXD2/PSC2-0	d44
4	RXD-2		URXD2/PSC2-1	d46
5	DCD-2		UDCD/PSC2-4	d52
6	CTS-2		UCTS2/PSC2-3	d50

USB Interface:

IMPORTANT NOTE:
The USB interface of the CRX01 can NOT be used with MPX5200 modules, since there is no known way to connect the CRX01's USB 2.0 Physical Layer Chip to the USB 1.1 interface of the MPC5200 processor!

The CRX01 contains two high speed USB host phys from SMSC according to USB specification Rev.2.0. The OTG function of the USB3300 devices is handled via jumper MSA for channel A and jumper MSB for channel B.

USB Connector Front view:



USB-A / USB-B Connector Pin out:

Pin:	USB-A	USB-B
1	Vbus+	Vbus+
2	D-	D-
3	D+	D+
4	GND	GND

OTG Jumper MSA/MSB:

Function	MSA/MSB	ID
A-Device	installed	0
B-Device	not installed	1

Jumper	USB-A	USB-B
MSA ---	ID=high	---
MSA 1-2	ID=low	---
MSB ---	---	ID=high
MSB 1-2	---	ID=low

USB Interconnection Channel A:

J10 / USB3300			ST2	
Signal	**Pin:**		**Signal**	**Pin:**
D0	24		MPH0-D0	c5
D1	23		MPH0-D1	c7
D2	22		MPH0-D2	c9
D3	21		MPH0-D3	c11
D4	20		MPH0-D4	c13
D5	19		MPH0-D5	c15
D6	18		MPH0-D6	c17
D7	17		MPH0-D7	c19
NXT	11		MPH0-NXT	c21
DIR	12		MPH0-DIR	c23
STP	13		MPH0-STP	c25
not connected	---		MPH0-PWFLT	c27
not connected	---		MPH0-PCTL0	c29
not connected	---		MPH0-PCTL1	c31
CLOCKOUT	14		MPH0-CLK	c33
RESET	9		HRST	a40
XI	28	OSC2-24MHz		
CPEN	3	MIC2025 (optional)		
ID	5	Jumper MSA		
DP	7	Connector USB-A.3		
DM	8	Connector USB-A.2		

USB Interconnection Channel B:

J12 / USB3300			ST2	
Signal	**Pin:**		**Signal**	**Pin:**
D0	24		MPH1-D0	c6
D1	23		MPH1-D1	c8
D2	22		MPH1-D2	c10
D3	21		MPH1-D3	c12
D4	20		MPH1-D4	c14
D5	19		MPH1-D5	c16
D6	18		MPH1-D6	c18
D7	17		MPH1-D7	c20
NXT	11		MPH1-NXT	c22
DIR	12		MPH1-DIR	c24
STP	13		MPH1-STP	c26
not connected	---		MPH1-PWFLT	c28
not connected	---		MPH1-PCTL0	c30
not connected	---		MPH1-PCTL1	c32
CLOCKOUT	14		MPH1-CLK	c34
RESET	9		HRST	a40
XI	28	OSC2-24MHz		
CPEN	3	MIC2025 (optional)		
ID	5	Jumper MSB		
DP	7	Connector USB-B.3		
DM	8	Connector USB-B.2		

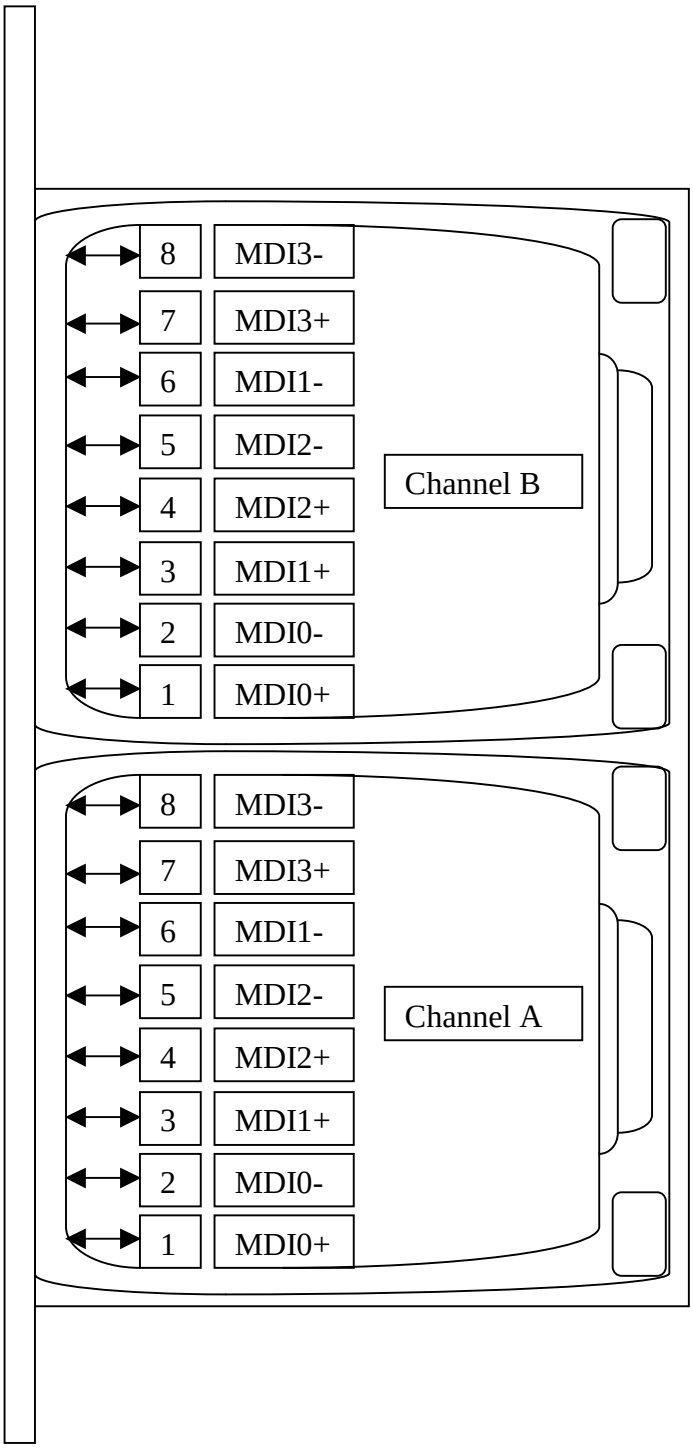
The Triple Speed Ethernet Phys:

The CRX01 uses two Marvell 88E1111 phys for Ethernet applications. They are able to work with 10, 100 or 1000Mbit transfer rate. The two Net-Phys are hardware configured with the following settings.

Marvel 88E1111 Hardware Configuration:

Function	Phy-A	Phy-B
Phy-Address	00000	00001
ENA-Pause	1	1
ANEG	1110	1110
HWCFG	1111	1111
DIS-FC	1	1
DIS-SLEEP	1	1
DIS_125	0	1
SEL-TWSI	0	0
INT-POL	1	1
75Ohm	1	1

The LAN RJ45 Connector Front view:



Signal Interconnection Ethernet Channel A:

J1 / 88E1111			ST2	
Signal	**Pin:**		**Signal**	**Pin:**
CLK125	K2		MII-GTXCK	a2
TXEN	E1		MII1-TXEN/ETH-0	a4
TXD0	F1		MII1-TXD0/ETH-1	a5
TXD1	G2		MII1-TXD1/ETH-2	a6
TXD2	G3		MII1-TXD2/ETH-3	a7
TXD3	H2		MII1-TXD3/ETH-4	a8
GTXCLK	E2		MII1-GXCK	a9
RXD0	B2		MII1-RXD0/ETH-12	a10
RXD1	D3		MII1-RXD1/ETH-13	a11
RXD2	C3		MII1-RXD2/ETH-14	a12
RXD3	B3		MII1-RXD3/ETH-15	a13
RXCLK	C1		MII1-RXCK/ETH-9	a14
RXDV	B1		MII1-RXDV/ETH-8	a15
CRS	B5		MII1-CRS/ETH-17	a16
TXD4	H1		MII1-TXD4	a17
TXD5	H3		MII1-TXD5	a18
TXD6	J1		MII1-TXD7	a19
TXD7	J2		MII1-TXD6	a20
TXER	F2		MII1-TXER/ETH-5	a21
RXD7	C5		MII1-RXD7	a22
RXD6	A2		MII1-RXD6	a23
RXD5	A1		MII1-RXD5	a24
RXD4	C4		MII1-RXD4	a25
RXER	D2		MII1-RXER/ETH-16	a26
COL	B6		MII1-COL/ETH-10	a27
TXCLK	D1		MII1-TXCK/ETH-11	a28
MDC	L3		MII-MDCK/ETH-6	a29
MDIO	M1		MII-MDIO/ETH-7	a31

Signal Interconnection Ethernet Channel B:

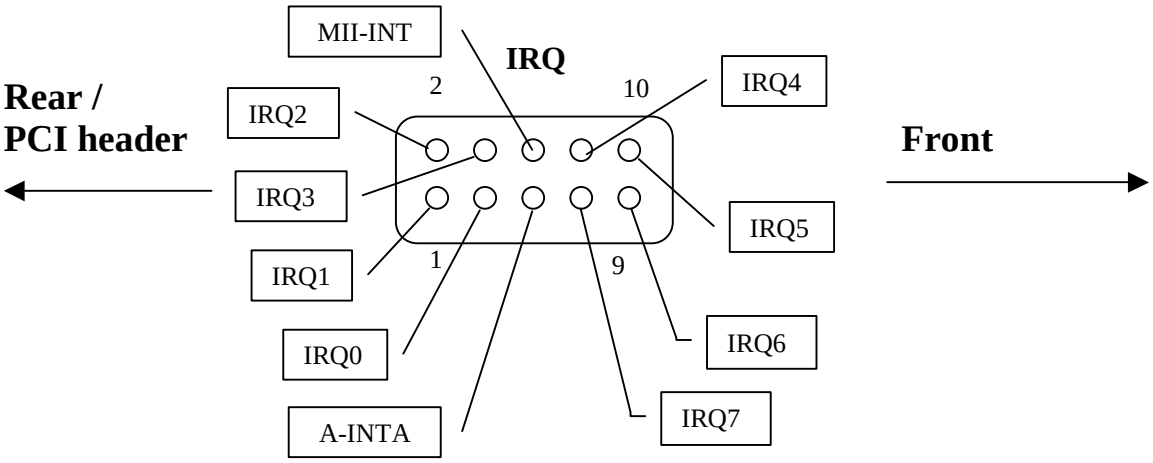
J2 / 88E1111			ST2	
Signal	**Pin:**		**Signal**	**Pin:**
CLK125	K2		MII-GTXCK	a2
TXEN	E1		MII2-TXEN	b4
TXD0	F1		MII2-TXD0	b5
TXD1	G2		MII2-TXD1	b6
TXD2	G3		MII2-TXD2	b7
TXD3	H2		MII2-TXD3	b8
GTXCLK	E2		MII2-GXCK	b9
RXD0	B2		MII2-RXD0	b10
RXD1	D3		MII2-RXD1	b11
RXD2	C3		MII2-RXD2	b12
RXD3	B3		MII2-RXD3	b13
RXCLK	C1		MII2-RXCK	b14
RXDV	B1		MII2-RXDV	b15
CRS	B5		MII2-CRS	b16
TXD4	H1		MII2-TXD4	b17
TXD5	H3		MII2-TXD5	b18
TXD6	J1		MII2-TXD7	b19
TXD7	J2		MII2-TXD6	b20
TXER	F2		MII2-TXER	b21
RXD7	C5		MII2-RXD7	b22
RXD6	A2		MII2-RXD6	b23
RXD5	A1		MII2-RXD5	b24
RXD4	C4		MII2-RXD4	b25
RXER	D2		MII2-RXER	b26
COL	B6		MII2-COL	b27
TXCLK	D1		MII2-TXCK	b28
MDC	L3		MII-MDCK/ETH-6	a29
MDIO	M1		MII-MDIO/ETH-7	a31

The Interrupt Link Field

The interrupt distribution of all module availabe interrupt lines is performed via the link area IRQ. The local interrupt sources from the onboard netphys, MII-INT, and the PCI connector, A-INTA, can be connected to any available IRQ input to the MPX module.

Attention ! Not all IRQs are usable with any MPX module !

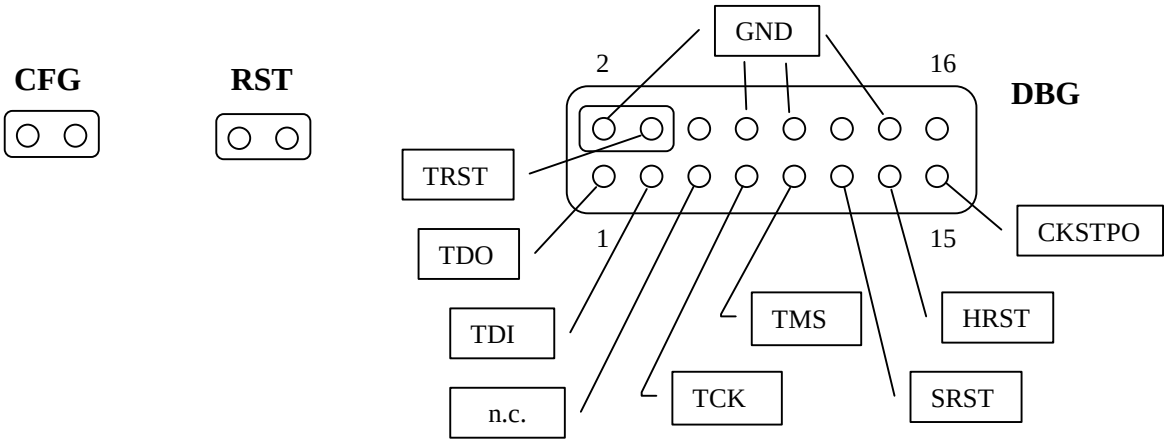
IRQ wrap header:



The JTAG/COP interface

The background debug port of the mounted processor module can be accessed via the connector DBG. In some cases, it is necessary to disable the module resident processor hardware configuration to work with a background debug tool. Therefore, jumper CFG can be installed, which connects the signal CFGE of module connector ST2-b29 to ground. During normal operation, link CFG should not be installed. If the JTAG interface of the mounted module is not used for debug purposes, it must be disabled. This is performed on some modules automatically, on others, the link RST must be set, or the TRST signal of connector DBG must be connected to ground by inserting a jumper in location 2-4.

The Debug Connector:



The Debug Connector Pin out:

DBG	Signal		Signal	DBG
Pin 1	TDO		GND	Pin 2
Pin 3	TDI		TRST#	Pin 4
Pin 5	n.c.		1K pull-up	Pin 6
Pin 7	TCK		n.c.	Pin 8
Pin 9	TMS		GND	Pin 10
Pin 11	SRST#		GND	Pin 12
Pin 13	HRST#		n.c.	Pin 14
Pin 15	CKSTPO#		GND	Pin 16

Normal Operation Module Overview:

Processor Module	Jumper Setting		
	CFG	**RST**	**DBG**
MPX8349 Rev.1	---	---	2-4
MPX5200 Rev.1	---	---	---

Debug Operation Module Overview:

Processor Module	Jumper Setting		
	CFG	**RST**	**DBG**
MPX8349 Rev.1	---	---	BDM
MPX5200 Rev.1	---	---	BDM

Module ST1-Connector Pin out:

Location:

c52	ST1	c1
d52	ST1	d1

a52	ST1	a1
b52	ST1	b1

c52	ST2	c1
d52	ST2	d1

a52	ST2	a1	
b52	ST2	b1	

LAD8	a2	a1	GND
LAD9	a4	a3	GND
LAD10	a6	a5	LAD0
LAD11	a8	a7	LAD1
LAD12	a10	a9	LAD2
LAD13	a12	a11	LAD3
LAD14	a14	a13	LAD4
LAD15	a16	a15	LAD5
GND	a18	a17	LAD6
GND	a20	a19	LAD7
LAD24	a22	a21	LAD16
LAD25	a24	a23	LAD17
LAD26	a26	a25	LAD18
LAD27	a28	a27	LAD19
LAD28	a30	a29	LAD20
LAD29	a32	a31	LAD21
LAD30	a34	a33	LAD22
LAD31	a36	a35	LAD23
ATA-ISOLATE	a38	a37	GND
DREQ0/ATA-DRQ	a40	a39	GND
DACK0/ATA-ACK	a42	a41	DONE0/ATA-IRQ
B-GNT0	a44	a43	B-REQ0
B-GNT1	a46	a45	B-REQ1
B-GNT2	a48	a47	B-REQ2
GND	a50	a49	B-RST
GND	a52	a51	B-PCICLK

LDP2	b2	b1	GND
LDP3	b4	b3	GND
LA30	b6	b5	LDP0
LA31	b8	b7	LDP1
LWE0	b10	b9	LA27
LWE1	b12	b11	LA28
LWE2	b14	b13	LA29
LWE3	b16	b15	LALE
LCS0	b18	b17	LGPL0/TSIZ1
LCS1	b20	b19	LGPL1/LWE
LCS2	b22	b21	LGPL2/LOE
LCS3	b24	b23	LGPL3/LTS
LCS4	b26	b25	LGPL4/LACK
LCS5	b28	b27	LGPL5/TSIZ2
LBCTL	b30	b29	LCLKE
GND	b32	b31	LCLK0
GND	b34	b33	DREQ1/ATA-IOR
DONE1/ATA-IOCHRDY	b36	b35	DACK1/ATA-IOW
A-INTA	b38	b37	A-M66EN
A-GNT0	b40	b39	A-REQ0
A-GNT1	b42	b41	A-REQ1
A-GNT2	b44	b43	A-REQ2
A-GNT3	b46	b45	A-REQ3
A-GNT4	b48	b47	A-REQ4
A-RST	b50	b49	GND
A-PCICLK	b52	b51	GND

Module ST1-Connector Pin out continued:

Location:

c52	ST1	c1
d52	ST1	d1

a52	ST1	a1
b52	ST1	b1

c52	ST2	c1
d52	ST2	d1

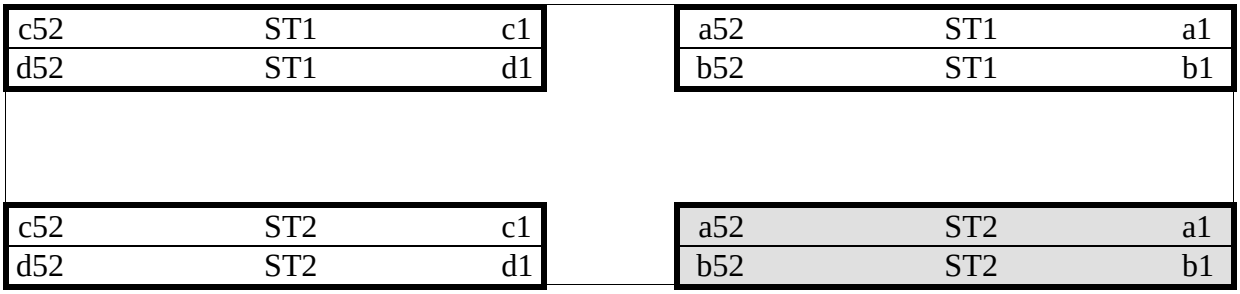
a52	ST2	a1
b52	ST2	b1

B-AD8/A-AD40	c2	c1	GND
B-AD9/A-AD41	c4	c3	GND
B-AD10/A-AD42	c6	c5	B-AD0/A-AD32
B-AD11/A-AD43	c8	c7	B-AD1/A-AD33
B-AD12/A-AD44	c10	c9	B-AD2/A-AD34
B-AD13/A-AD45	c12	c11	B-AD3/A-AD35
B-AD14/A-AD46	c14	c13	B-AD4/A-AD36
B-AD15/A-AD47	c16	c15	B-AD5/A-AD37
GND	c18	c17	B-AD6/A-AD38
GND	c20	c19	B-AD7/A-AD39
B-CBE1/A-CBE5	c22	c21	B-CBE0/A-CBE4
B-DVSL/A-ACK64	c24	c23	B-FRME/A-REQ64
B-PERR	c26	c25	B-IRDY
B-SERR	c28	c27	B-TRDY
B-PAR/A-PAR64	c30	c29	B-STOP
B-CBE3/A-CBE7	c32	c31	B-CBE2/A-CBE6
B-AD24/A-AD56	c34	c33	GND
B-AD25/A-AD57	c36	c35	GND
B-AD26/A-AD58	c38	c37	B-AD16/A-AD48
B-AD27/A-AD59	c40	c39	B-AD17/A-AD49
B-AD28/A-AD60	c42	c41	B-AD18/A-AD50
B-AD29/A-AD61	c44	c43	B-AD19/A-AD51
B-AD30/A-AD62	c46	c45	B-AD20/A-AD52
B-AD31/A-AD63	c48	c47	B-AD21/A-AD53
GND	c50	c49	B-AD22/A-AD54
GND	c52	c51	B-AD23/A-AD55

A-AD8	d2	d1	GND
A-AD9	d4	d3	GND
A-AD10	d6	d5	A-AD0
A-AD11	d8	d7	A-AD1
A-AD12	d10	d9	A-AD2
A-AD13	d12	d11	A-AD3
A-AD14	d14	d13	A-AD4
A-AD15	d16	d15	A-AD5
GND	d18	d17	A-AD6
GND	d20	d19	A-AD7
A-CBE1	d22	d21	A-CBE0
A-DVSL	d24	d23	A-FRME
A-PERR	d26	d25	A-IRDY
A-SERR	d28	d27	A-TRDY
A-PAR	d30	d29	A-STOP
A-CBE3	d32	d31	A-CBE2
A-AD24	d34	d33	GND
A-AD25	d36	d35	GND
A-AD26	d38	d37	A-AD16
A-AD27	d40	d39	A-AD17
A-AD28	d42	d41	A-AD18
A-AD29	d44	d43	A-AD19
A-AD30	d46	d45	A-AD20
A-AD31	d48	d47	A-AD21
GND	d50	d49	A-AD22
GND	d52	d51	A-AD23

Module ST2-Connector Pin out:

Location:



MII-GTXCKI	a2	a1	GND
MII1-TXEN/ETH-0	a4	a3	GND
MII1-TXD1/ETH-2	a6	a5	MII1-TXD0/ETH-1
MII1-TXD3/ETH-4	a8	a7	MII1-TXD2/ETH-3
MII1-RXD0/ETH-12	a10	a9	MII1-GXCK
MII1-RXD2/ETH-14	a12	a11	MII1-RXD1/ETH-13
MII1-RXCK/ETH-9	a14	a13	MII1-RXD3/ETH-15
MII1-CRS/ETH-17	a16	a15	MII1-RXDV/ETH-8
MII1-TXD5	a18	a17	MII1-TXD4
MII1-TXD6	a20	a19	MII1-TXD7
MII1-RXD7	a22	a21	MII1-TXER/ETH-5
MII1-RXD5	a24	a23	MII1-RXD6
MII1-RXER/ETH-16	a26	a25	MII1-RXD4
MII1-TXCK/ETH-11	a28	a27	MII1-COL/ETH-10
GND	a30	a29	MII-MDCK/ETH-6
GND	a32	a31	MII-MDIO/ETH-7
CKSTI	a34	a33	JTMS
CKSTO	a36	a35	JTDI
KRST	a38	a37	JTDO
HRST	a40	a39	JTCK
SRST	a42	a41	JTRST
IRQ3	a44	a43	IRQ0
IRQ4	a46	a45	IRQ1
IRQ5	a48	a47	IRQ2
IRQ6	a50	a49	GND
IRQ7	a52	a51	GND

spare	b2	b1	GND
MII2-TXEN	b4	b3	GND
MII2-TXD1	b6	b5	MII2-TXD0
MII2-TXD3	b8	b7	MII2-TXD2
MII2-RXD0	b10	b9	MII2-GXCK
MII2-RXD2	b12	b11	MII2-RXD1
MII2-RXCK	b14	b13	MII2-RXD3
MII2-CRS	b16	b15	MII2-RXDV
MII2-TXD5	b18	b17	MII2-TXD4
MII2-TXD6	b20	b19	MII2-TXD7
MII2-RXD7	b22	b21	MII2-TXER
MII2-RXD5	b24	b23	MII2-RXD6
MII2-RXER	b26	b25	MII2-RXD4
MII2-TXCK	b28	b27	MII2-COL
GND	b30	b29	CFGE
GND	b32	b31	PRST
GTM-IO8	b34	b33	GTM-IO0/TMR-0
GTM-IO9	b36	b35	GTM-IO1/TMR-1
GTM-IO10	b38	b37	GTM-IO2/TMR-2
GTM-IO11	b40	b39	GTM-IO3/TMR-3
GTM-IO12	b42	b41	GTM-IO4/TMR-4
GTM-IO13	b44	b43	GTM-IO5/TMR-5
GTM-IO14/GPIO-WKUP6	b46	b45	GTM-IO6/TMR-6
GTM-IO15/GPIO-WKUP7	b48	b47	GTM-IO7/TMR-7
spare	b50	b49	GND
spare	b51	b52	GND

Module ST2-Connector Pin out continued:

Location:

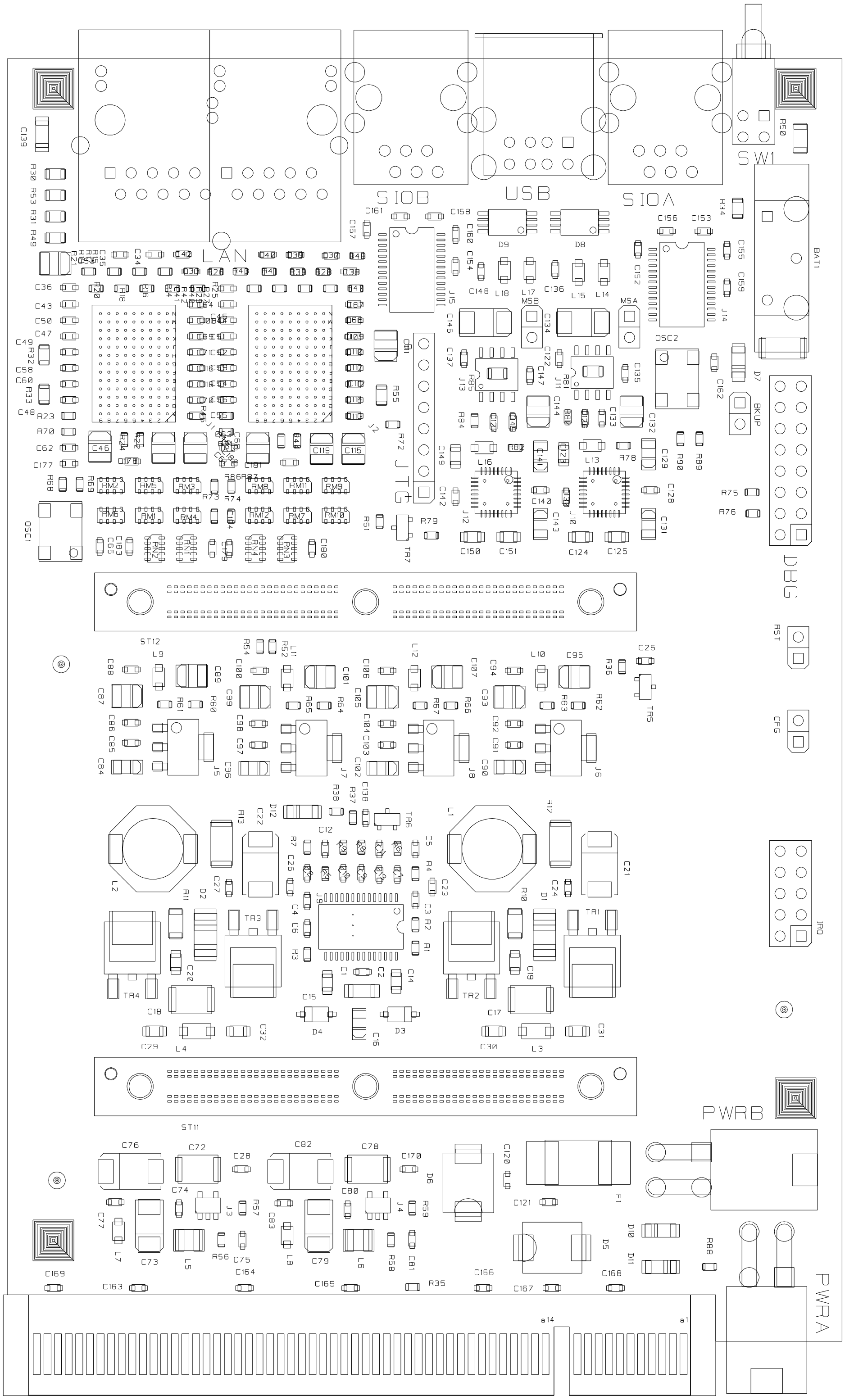
c52	ST1	c1		a52	ST1	a1
d52	ST1	d1		b52	ST1	b1

c52	ST2	c1		a52	ST2	a1
d52	ST2	d1		b52	ST2	b1

VEE Core	c2	c1	GND
VFF RAM	c4	c3	GND
MPH1-D0	c6	c5	MPH0-D0
MPH1-D1	c8	c7	MPH0-D1
MPH1-D2	c10	c9	MPH0-D2
MPH1-D3	c12	c11	MPH0-D3
MPH1-D4	c14	c13	MPH0-D4
MPH1-D5	c16	c15	MPH0-D5
MPH1-D6	c18	c17	MPH0-D6
MPH1-D7	c20	c19	MPH0-D7
MPH1-NXT	c22	c21	MPH0-NXT
MPH1-DIR	c24	c23	MPH0-DIR
MPH1-STP	c26	c25	MPH0-STP
MPH1-PWFLT	c28	c27	MPH0-PWFLT
MPH1-PCTL0	c30	c29	MPH0-PCTL0
MPH1-PCTL1	c32	c31	MPH0-PCTL1
MPH1-CLK	c34	c33	MPH0-CLK
GND	c36	c35	GND
GND	c38	c37	GND
CS0E	c40	c39	STDBY
VDD	c42	c41	VDD
VDD	c44	c43	VDD
VDD	c46	c45	VDD
VDD	c48	c47	VDD
VDD	c50	c49	VDD
VDD	c52	c51	VDD

USB1-0/FEC-TXCK	d2	d1	GND
USB1-1/FEC-TXEN	d4	d3	GND
USB1-2/FEC-TXD1	d6	d5	PSC3-0/FEC-TXD0
USB1-3/FEC-TXD3	d8	d7	PSC3-1/FEC-TXD2
USB1-4/FEC-CLSN	d10	d9	PSC3-2/FEC-TXER
USB1-5/FEC-CRSN	d12	d11	PSC3-3/FEC-RXER
USB1-6/FEC-RXD1	d14	d13	PSC3-4/FEC-RXD0
USB1-7/FEC-RXD3	d16	d15	PSC3-5/FEC-RXD2
USB1-8/FEC-RXDV	d18	d17	SPI-MOSI/PSC3-6
USB1-9/FEC-RXCK	d20	d19	SPI-MISO/PSC3-7
GND	d22	d21	SPI-SEL/PSC3-8
GND	d24	d23	SPI-CLKPSC3-9
spare	d26	d25	spare
spare	d28	d27	spare
spare	d30	d29	spare
spare	d32	d31	spare
UTXD1/PSC1-0	d34	d33	I2C1-SDA/I2C-1
URXD1/PSC1-1	d36	d35	I2C1-SCL/I2C-0
URTS1/PSC1-2	d38	d37	I2C2-SDA/I2C-3
UCTS1/PSC1-3	d40	d39	I2C2-SCL/I2C-2
UDCD/PSC1-4	d42	d41	PSC6-0/UTXD3
UTXD2/PSC2-0	d44	d43	PSC6-1/URXD3
URXD2/PSC2-1	d46	d45	PSC6-2/URTS3
URTS2/PSC2-2	d48	d47	PSC6-3/UCTS3
UCTS2/PSC2-3	d50	d49	GND
UDCD/PSC2-4	d52	d51	GND

Layout Component Side



Location of Jumpers and Switches