MicroSys

User's Manual

CPC45 Rev. 4

1st edition

Declaration of Conformity

We, Manufacturer
MicroSys Electronics GmbH
Mühlweg 1
D-82054 Sauerlach
Germany

declare that the product

CPC45

is in conformity with:

EN 50081-1 Generic emission standard
EN 50082-1 Generic immunity standard

in accordance with **89/336 EEC-EMC** Directive.

We also declare the conformity of the above mentioned product with the actual required safety standards in accordance with Low Voltage Directive **73/23 EEC**.

Date:

Signature:

Position: General Manager

Edition

	Date:	Ident-Nr.:	Released:
Manual Adapted to Rev.4 PCB. Chapter 6.4.4 and 6.6.3: Hardware revision register. description adtapted to revision 4.	13.08.2004	EW286MA-04AA	
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1. Introduction

1.1 Short Description

The **Double Euro** CompactPCI board **CPC45** is powered by the Motorola PowerPC **MPC8245**.

It features a **64 bit** wide **SODIMM SDRAM** module, a **64 bit** wide **8 MByte Flash** memory bank and a 32 pin 8 bit wide JEDEC socket for multiple ROM types. The CPC45 offers a **32 bit** wide **SRAM** area with battery backup.

The four onboard serial ports are handled via the MPC8245 internal SMC ports and an additional **UART** with **16 Byte R/W-FIFO**.

The I^2C-Interface of the MPC8245 controls a **512Byte EEPROM,** a **RTC** with battery backup and a **System Monitor** for supply voltage and temperature supervision.

The **PCI Interface** of the MPC8245 controls the local PCI bus, which contains a **LAN interface**, a **Compact-Flash-Card controller**, a **peripheral interface target bridge** and a **PCI to PCI** bridge for the **Compact-PCI** connection.

The complete board is implemented in **CMOS technology**, which allows for a power consumption as low as: **3.3V / xxW @ 300 MHz** CPU speed.

The 3.3 volt board supply voltage is protected by a transient suppresser diode against overvoltage or wrong polarity.

The CPC45 conforms to the Compact PCI specification **PICMG 2.0 R3.0**.

1.2 Options

- different DRAM sizes
- different FLASH memory sizes
- different SRAM memory sizes

1.3 Specifications

The power requirements for the CPC45 board are shown in the following table. The power consumption of the optionally used extension boards must be added to the given values.

Power Requirements:

+3.3V, +5%/-2.5%,	
+5V, +5%/-2.5%,	
+12V, +5%/-2.5%	
-12V, +5%/-2.5%	

Environmental Requirements:

Operating Temperature	0 ° C to +70 ° C
Relative Humidity	0 to 95 % (non-condensing)
Storage Temperature	-40 ° C to + 85 ° C

1.4 Related Documentation

The following manuals are applicable to the CPC45

- CompactPCI Specification Manual PICMG 2.0 R3.0
- MPC8245 RISC Microprocessor User's Manual
- I82259 Fast Ethernet PCI Controller
- D6729 PCI PC-Card Controller
- PCI9030 SmarTarget I/O Accelerator
- ST16C2550 Dual UART Data Sheet
- PDSP1881 Programmable Alphanumeric Display
- LM81 System Hardware Monitor
- PCF8563 Real-time Clock
- 24C164 EEPROM Data Sheet
- SDRAM SODIMM Module Data Sheet
- Intel 28F160F3 and 28F160C3 Flash Data Sheet

2. Delivery

2.1 Items shipped with this unit

- User's Manual CPC45 Hardware
- MicroSys shipping carton

ATTENTION: STATIC DISCHARGE CAN DESTROY UNIT

2.2 Hints for unpacking, handling and storing

- Avoid touching areas of integrated circuitry.
- Unit should only be placed on a static-free conductive surface
- Unit must only be transported using anti-static bags or MicroSys shipping carton
- Packing should be saved if unit needs to be reshipped or returned
- When the unit needs to be stored, it should be placed in a moistfree, dustfree environment. The storage temperatures and humidity specifications are shown in chapter 1

3. Installation

3.1 Items required for CPC45 installation

For installation of the CPC45, the following items are required.

- Card cage or housing
- Compact PCI motherboard
- Adequate rated power supply

3.2 Points to be observed

Before the unit is inserted into the card cage, the following points should be observed.

- Unit requires +3.3V (+5 %, -3 %),
- Unit requires +5V (+5 %, -3 %),
- Be sure voltage is of correct polarity.
- Unit should only be inserted into, and removed from card cage when power is off.
- Any modules must only be inserted or removed during power off.
- Check default jumper or switch setting.

The card cage must be well ventilated. The operating temperature must never exceed it's specified range. Never use the board without forced cooling!

GUARANTEE IS VOID IF UNIT IS OPERATED OUT OF IT'S SPECIFICATIONS!

4. Board Overview

4.1 Features CPC45

Board Format:	double eurocard format
Main Processor:	MPC8245 with PowerPC 603 Core 64 bit peripheral bus 32 bit PCI 2.2 Bus Interface 16 Kbyte instruction cache 16 Kbyte data cache onchip floating point unit 300MHz CPU core clock rate two RS232 serial I/O channels
Dynamic RAM:	144 pin SODIMM SDRAM module socket 128 MByte capacity 64 bit data bus width Serial Presence Detect (SPD)
Flash Memory:	8 MByte capacity 64 bit data bus width BGA or TSOP option
Ethernet Interface:	I82259 Fast Ethernet Controller 10/100BaseT Interface two status LEDs local PCI located
CF-Card Interface:	D6729 PC-Card Controller local PCI located
I/O PCI Interface:	PCI9030 I/O Accelerator SRAM interface controller UART interface controller Display interface controller local PCI located
C-PCI Interface:	21150 PCI-to-PCI bridge 33MHz, 3.3V primary bus 33MHz, 5V secondary bus
Static RAM:	512Kbyte or 2 MByte capacity 32 bit data bus width local PCI located via PCI9030 data backup with onboard gold cap
Serial Interface:	ST16C2550 dual UART 16 byte transmit FIFO 16 byte receive FIFO local PCI located via PCI9030
Front Display:	PDSP1881 8-digit display alphanumeric programmable display local PCI located via PCI9030

EEPROM:	2KByte I^2C serial access device
System Supervisor:	LM81 hardware monitor for temperature and voltage control I^2C serial access device voltage programmable reset level
Real Time Clock:	PCF8563 with time & date function I^2C serial access device backup function with onboard supply
Data backup:	short time backup via service free gold cap external backup via external standby line
Front panel LEDs:	two user programmable LEDs two board status LEDs two network status LEDs
Front panel Keys:	RESET/ABORT key Key I/Key II for user applications
System controller:	full Compact PCI slot 1 functions
Compact PCI interface:	according to PICMG 2.0 R3.0

5. Addressmap CPC45

MPC8245 local bus devices	Base	End	Select	Size
SDRAM Bank	$0000 0000	$01FF FFFF	local CS0	64Bit
Flash Memory Bank 1	$FF00 0000	$FF7F FFFF	local RCS1	64Bit
Boot Socket	$FF80 0000	$FFFF FFFF	local RCS0	8Bit

local PCI controlled devices	Memory-Base	I/O-Base	ID-Select	Size
PCI-2050 PCI to PCI Bridge	---	---	AD16	32Bit
LAN I82259 Ethernet Controller	$C040 1000* $C042 0000*	$FE10 40C0*	AD15	32Bit
D6729 CF-Card Controller	$8100 0000*	$FE10 4080*	AD14	32Bit
PCI9030 I/O Accelerator	$C000 4000*	$FE10 4000*	AD13	32Bit
MPC8245	---	---	AD12	32Bit

PCI9030 controlled devices	Base	End	Select	Size
SRAM	$8000 0000	$801F FFFF	CS0	32Bit
ST16C2550 Channel A	$8020 0000	$8020 0007	CS1	8Bit
ST16C2550 Channel B	$8040 0000	$8040 0007	CS2	8Bit
Interrupt Enable Register I	$8060 0000	$8060 0000	CS3	8Bit
Interrupt Status Register I	$8060 0001	$8060 0001	CS3	8Bit
Interrupt Enable Register II	$8060 0002	$8060 0002	CS3	8Bit
Interrupt Status Register II	$8060 0003	$8060 0003	CS3	8Bit
Board Control Register	$8060 0004	$8060 0004	CS3	8Bit
Board Status Register	$8060 0005	$8060 0005	CS3	8Bit
Watchdog Start / Prestop / Stop Port	$8060 0006	$8060 0006	CS3	8Bit
ispLSI Revision Register 1	$8060 0008	$8060 0008	CS3	8Bit
ispLSI Revision Register 2	$8060 0009	$8060 0009	CS3	8Bit
Display Data Register	$8060 0040	$8060 0040	CS3	8Bit
Display Flash Register	$8060 0060	$8060 0060	CS3	8Bit

I^2C controlled devices	write	read
24C164 EEPROM	$B0-$BE	$B1-$BF
LM81 System Hardware Monitor	$58	$59
PCF8563 Real Time Clock	$A2	$A3
SODIMM Socket with SPD protection register	$60	$61
SODIMM Socket with SPD memory range	$A0	$A1
I82559 Fast Ethernet Controller	programmable	programmable

(*)The given addresses are set by the **VxWorks** PCI-BIOS autoscan function

6. Functional Description

6.1 The MPC8245 Processor

The CPC45 uses the MPC8245 PowerPC RISC microprocessor from Motorola. It can be configured for different CPU core and bus speed versions. The MPC8245 contains a 603e compatible core with 16 Kbyte data cache and 16 Kbyte instruction cache. It works on 3.3 volts bus supply and with 2.0 volts core supply voltage. The processor works with CPU clock rates from 99 up to 300MHz. The according local bus clock rate varies from 33 to 100MHz, while the PCI bus clock is driven by a **33MHz** oscillator. The desired clock configuration can be adjusted via the soldering link area PLL according to the following table.

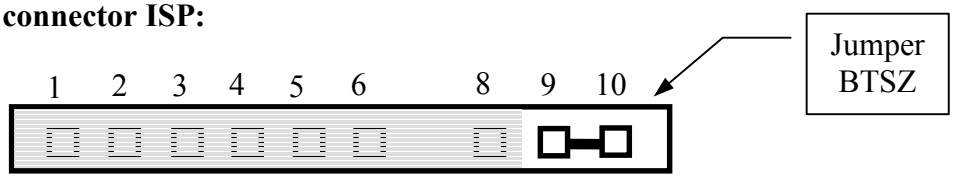
PLL					MPC8245 - 300MHz Type		
1-2	3-4	5-6	7-8	9-10	PCI-Clock	Local Bus Clock	CPU-Clock
x	x	x	x	x	33MHz	99MHz	247.5MHz
x	**x**	**x**	**x**	**---**	**33MHz**	**99MHz**	**297MHz**
x	x	x	**---**	x	33MHz	33MHz	148.5MHz
x	x	---	x	x	33MHz	66MHz	132MHz
x	---	x	---	x	33MHz	66MHz	297MHz
x	**---**	---	x	x	33MHz	66MHz	165MHz
x	---	---	---	x	33MHz	66MHz	198MHz
---	x	x	x	x	33MHz	99MHz	198MHz
---	x	---	x	x	33MHz	66MHz	231MHz
---	x	---	**---**	x	33MHz	66MHz	264MHz
---	**---**	x	x	x	33MHz	82.5MHz	247.5MHz

(x = link installed / --- link not installed)

The local data bus is configured for **64 bit** for the **SODIMM** SDRAM module connected to **CS0 and CS1.** The **64 bit Flash** memory bank is connected to **RCS0** or **RCS1** and the **8 bit JEDEC** socket uses **RCS1** or **RCS0,** depending on the state of jumper **BTMD** and **BTSZ .** The jumper **BTSZ is a part of the wrap connector ISP**. No other connections must be made to this connector. All other select lines are not used on the local bus side of the MPC8245.

BTMD	Function	BTSZ
Pin 3-5	CS0 connected to 8 bit socket	ISP-Pin 9-10
Pin 4-6	CS1 connected to 64 bit Flash	ISP-Pin 9-10
Pin 3-4	CS0 connected to 64 bit Flash	open
Pin 5-6	CS1 connected to 8 bit socket	open

Pinout of wrap connector ISP:



Attention !

The MPC8245 bus configuration allows for an **8 bit** device **only** at **CS0**, while the CS1 controlled device must have always the same bus size than the SDRAM configuration. The SDRAM onboard the CPC45 has got a 64 bit bus width, i.e. the memory connected to CS1 must have also a 64 bit data bus. In case the 64 bit flash is controlled by CS0, **the 8 bit socket cannot be used** for linear data access together with the CS1 select line.

The **JTAG** interface of the CPC45 can be used via the 16 pin standard wrap connector JTAG according to following table.

JTAG	Signal		Signal	JTAG
Pin 1	TDO		n.c.	Pin 2
Pin 3	TDI		TRST*	Pin 4
Pin 5	10K pull-up		2K2 pull-up	Pin 6
Pin 7	TCK		CKSTI	Pin 8
Pin 9	TMS		n.c.	Pin 10
Pin 11	SRST*		n.c.	Pin 12
Pin 13	DRST*		n.c.	Pin 14
Pin 15	10K pull-up		GND	Pin 16

6.1.1 Board specific MPC8245 register values

Memory Control Configuration Register 1: **$04680000 (64MB SODIMM)**
Memory Control Configuration Register 1: **$04680002 (128MB SODIMM)**

BIT Location:	Binary Value	Result:	Description:
ROMNAL	0000	30ns + 0x10ns	Flash Burst Cycle Length
ROMFAL	01000	30ns + 8x10ns	Flash Initial Cycle Length
DBUS-Size	11	64 Bit	SDRAM & Flash Bank A / B
ROM Burst	0	enable	Flash Burst Mode
MEMGO	(1)*	enable	Set to enable RAM interface
SREN	0	disable	SDRAM self refresh during sleep
RAM Type	0	SDRAM	FPM/EDO or SDRAM mode
PCKEN	0	disable	Parity Check
DRAM Bank 7	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 6	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 5	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 4	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 3	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 2	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 1	00	12 rows / 4 banks	SDRAM row address bit count
DRAM Bank 0	00	12 rows / 4 banks	SDRAM row address bit count **(64MB)**
DRAM Bank 0	10	12 rows / 4 banks	SDRAM row address bit count **(128MB)**

*** this bit must be set after complete configuration setting by a read modify write sequence !**

Memory Control Configuration Register 2: **$000017D0 (64MB SODIMM)**
Memory Control Configuration Register 2: **$00000BB0 (128MB SODIMM)**

BIT Location:	Binary Value	Result:	Description:
TS wait timer	000	2x10ns	Flash data out disable time
AS ARISE time	0000	not used	AS falling edge of port X interface
AS AFALL time	0000	not used	AS rising edge of port X interface
ECC / Parity	0	not used	ECC or Parity Check mode
Write Parity Check	0	disabled	write parity error report function
Inline Parity Check	0	disabled	inline parity/ECC error report function
look aside ECC logic	0	disabled	FPM/EDO ram ECC function
EDO option	0	disabled	DRAM Extended data out
Refresh Interval	00010111110100	0x17D0	Clock Cycles between CBR Refreshes **(64MB)**
Refresh Interval	00001011101100	0x2EC	Clock Cycles between CBR Refreshes **(128MB)**
open page mode	0	4 open pages	3 or 4 open page DRAM mode
RMW parity	0	disabled	read modify write parity mode

Memory Control Configuration Register 3: **$x82000000**

BIT Location:	Binary Value	Result:	Description:
Burst to precharge	1000	. . . . 1000 . .	SDRAM open page time, middle-bits
refresh to active	0010	2x10ns	SDRAM refresh to activate command
	00000000	all 0's	reserved
	00000000	all 0's	reserved
	00000000	all 0's	reserved

Memory Control Configuration Register 4: **$25102222**

BIT Location:	Binary Value	Result:	Description:
precharge to active	0010	2x10ns	SDRAM precharge to activate delay
active to precharge	0101	5x10ns	SDRAM activate to precharge delay
Burst Mode	0	4 beats	4 or 8 beat burst mode
INLINE	0	disabled	inline ECC/parity function
extended ROM	0	enabled	256MByte space enabled
register mode	1	enabled	clocked data interface
burst to precharge	00	 00	SDRAM open page time, ls-bits
reserved	xx		read value and write back
registered DIMM	0	disabled	normal SDRAM mode
CAS latency	010	2x10ns	transferred to SDRAM at power up
sequential mode	0	enabled	sequential or interleaved mode
SDRAM burst length	010	4 beats	transferred to SDRAM at power up
active to read/write	0010	2x10ns	SDRAM activate to r/w command
burst to precharge	0010	0010	SDRAM open page time, ms-bits

Clock Driver Control Register: **$FC28**

BIT Location:	Binary Value	Result:	Description:
PCI clock (0-4)	111111	enable	all PCI clocks disabled
reserved	00		
power up config.	x		read value and write back
SDRAM clock (0-3)	0001	enable	SDRAM clock 0-2 active, 3 inactive
reserved	000		

Output Driver Control Register: **$47**

BIT Location:	Binary Value	Result:	Description:
DRV PCI	0	40 Ohms	PCI drive capability
DRV STD	2	20 Ohms	non PCI drive capability
DRV MEM CTRL	00	40 Ohms	memory driver capability
DRV PCI CLK	01	40 Ohms	PCI clock drive capability
reserved	11		

Processor Interface Configuration Register 1: **$FF141BD8**

BIT Location:	Binary Value	Result:	Description:
reserved	11111111		read value and write back
reserved	00	0	must be cleared
reserved	0		read value and write back
RCS0 state	read only	local ROM	power up reset configuration
reserved	x		read value and write back
processor type	read only	10	host processor type is 603e
reserved	xxxx		read value and write back
flash write enable	1	enabled	flash write mode
MCP enable	1	enabled	machine check assertion
reserved	x		read value and write back
DPARK	1	disabled	the data bus will not be parked to CPU
TBEN	1	enabled	processor core decrementer enabled
no bus check	1	disabled	flash bus write size check
store gathering	1	enabled	PCI buffer function
big endian mode	0	enabled	little or big endian mode
reserved	1		must be set to 1
APARK	1	enabled	the address bus will be parked to CPU
PCI memory reads	0	disabled	no speculative PCI reads from memory
reserved	xx		read value and write back

Processor Interface Configuration Register 2: **$04000000**

BIT Location:	Binary Value	Result:	Description:
reserved	xx		read value and write back
PCI serialize flag	0	disabled	no serialized PCI configuration writes
reserved	x		read value and write back
no snoop enable	0	disabled	PCI to local memory snoop enabled
ROM remapping	1	local	all ROM/Flash accesses on local bus
Flash write lock	0	disabled	Flash writes are enabled
reserved	xxxxx		read value and write back
snoop wait states	00	0 waitsate	snoop waitstate count
reserved	xxxxxxxxxxxx x		read value and write back
address phase waits	00	0 waitstate	address phase waitstate count
reserved	xx		read value and write back

For detailed chip information see
Technical manual MPC8245

6.2 Memory

6.2.1 The DRAM Area

The CPC45 is able to carry a 144 pin SODIMM SDRAM module with SPD via EEPROM. The module socket is directly controlled by the CS0 and CS1 select lines of the MPC8245. The SDRAM data port is 64 bits wide and no parity check is performed. The SPD responds on the I^2C bus at the access address $A1 or $A0 for read or write operations. The protection register access address of the SPD is located at $61 and $60. The pins of the SODIMM socket are controlled by the MPC8245 according to following table.

SDRAM	MPC8245	Description
A0-A9	SDMA0-SDMA9	address
A10/AP	SDMA10	address/auto precharge
A11-A13	SDMA11-SDMA13	address
BA0	SDBA0	bank address 0
BA1	SDBA1	bank address 1
CLK0	SDRAM-CLK-0	clock
CLK1	SDRAM-CLK-1	clock
CKE0-CKE1	CLKE	clock enable
DQM0-DQM7	SDQM0-SDQM7	data I/O mask
RAS	SDRAS	row address strobe
CAS	SDCAS	column address strobe
CS0	RAS/CS-0	chip select
CS1	RAS/CS-1	chip select
WE	WE	write enable
SCL	SCL	I^2C clock
SDA	SDA	I^2C data

For detailed information about the SDRAM specification, please refer to the according SODIMM data sheet.

6.2.2 The Flash Memory

The flash memory area of the CPC45 consists of 4 devices (Intel 28F160F3T or 28F160C3T) with a total capacity of 8Mbyte. The data bus is 64bits wide and no parity check is performed. The Flash bank is controlled via the RCS0 or RCS1 line of the MPC8245, depending on the jumper setting of BTMD and BTSZ. The data lanes of all devices are swapped according to the necessary endian conversion. The WAIT pin is not connected and left floating. The ADV pin is connected to ground for non burst mode operation.
If the soldering link FA is set to position 1-2, the ADV pin is connected to the CE pin for optional burst mode (28F160F3T devices only!).
The pins of the Flash devices are controlled by the MPC8245 according to following table.

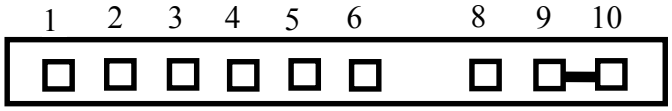
Flash Bank	MPC8245	Description
A0-A10	SDMA0-SDMA10	address
A11	SDBA0	address
A12-A19	AR7-AR0	address
A20	SDBA1	address
CLK	SDRAM-CLK-2	clock
CE	RCS0 or RCS1	chip select
OE	FOER	output enable
ADV	RCS0 or GND	address valid
WE	WE via ispLSI	write enable
RST	FRST	hard reset
WP	via ispLSI	write protect
D0-D15	D15-D0	endian swapped data lanes

In case the 64 bit Flash is controlled by the RCS0 line, i.e. it is configured as boot device, the 8 bit wide socket cannot be used, because the MPC8245 supports an 8 or 64 bit device on RCS0 only, while the RCS1 select is fixed to the size of the SDRAM bus width.

Boot device jumper setting:

BTMD	Function	BTSZ
Pin 3-5	CS0 connected to 8 bit socket	ISP-Pin 9-10
Pin 4-6	CS1 connected to 64 bit Flash	ISP-Pin 9-10
Pin 3-4	CS0 connected to 64 bit Flash	open
Pin 5-6	CS1 connected to 8 bit socket	open

Pinout of wrap connector ISP:



To protect the Flash memory contents against unattended write cycles, a security function has been implemented.

The (B)oard (C)ontrol (R)e(G)ister at location PCI9030-CS3+$05 allows a complete protection against all write accesses to the flash devices. The BCRG contains four protection bits, two for the bank write line (WE) and two for the write protect pin (WP) of the flash devices. The BCRG can be read back for verification. After a reset, these bits are set to low and the write protect mode is activated.

BCRG @ $04	D7	D6	**D5**	**D4**	D3	D2	**D1**	**D0**
read/write	WRSE	KRSE	**FWRE**	**FWPT**	LED2	LED1	**FWRE**	**FWPT**
reset	0	0	**0**	**0**	0	0	**1**	**1**
Flash-Bank write disable	x	x	**0**	**x**	x	x	**1**	**x**
Flash-Bank write enable	x	x	**1**	**x**	x	x	**0**	**x**
Flash-Bank WP pin low	x	x	**x**	**0**	x	x	**x**	**1**
Flash-Bank WP pin high	x	x	**x**	**1**	x	x	**x**	**0**

For detailed chip information see Technical manual of Intel 28F160 flash memory products.

6.2.3 The Boot Socket

The boot socket of the CPC45 consists of a 32 pin JEDEC compatible 600mil standard socket for 8 bit wide **ROMs**, **PROMs**, **EPROMs** or **Flash 3.3V devices**. The device type selection is made by the 3 soldering links BA, BB and BC. The socket can be controlled via the RCS0 or the RCS1 line of the MPC8245. The selection between both CS-lines is performed via jumper BTMD. If the links are set to BTMD(3-5) and BTMD(4-6), the socket is connected to the CS0 line, while the 64 bit flash memory is controlled via the CS1 line of the MPC8245. In addition, the jumper BTSZ (ISP 9-10) must be set when 8Bit socket is configured as boot device. The data lanes are swapped according to the necessary endian conversion. The pins of the socket are controlled by the MPC8245 according to following table.

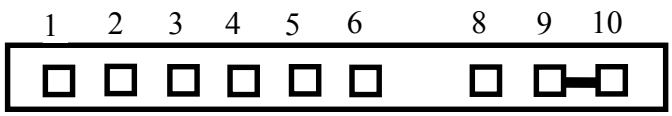
Boot Socket	MPC8245	Description
A0-A10	SDMA0-SDMA10	address
A11	SDBA0	address
A12-A16	AR7-AR3	address
A17/Vdd	Vdd/AR2	via link BB
A18/WE	Vdd/AR1/FLWE	via link BC
A19/VPP	Vdd/AR0/AR1	via link BA
CE	RCS0/RCS1	via link BTMD
OE	FOER	output enable
D0-D7	D7-D0	endian swapped data lanes

In case the 8 bit socket is not controlled by the RCS0 line, it cannot be used, because the MPC8245 supports an 8 or 64 bit device on RCS0 only, while the RCS1 select is fixed to the size of the SDRAM bus width, which is 64 bits.

Boot device jumper setting:

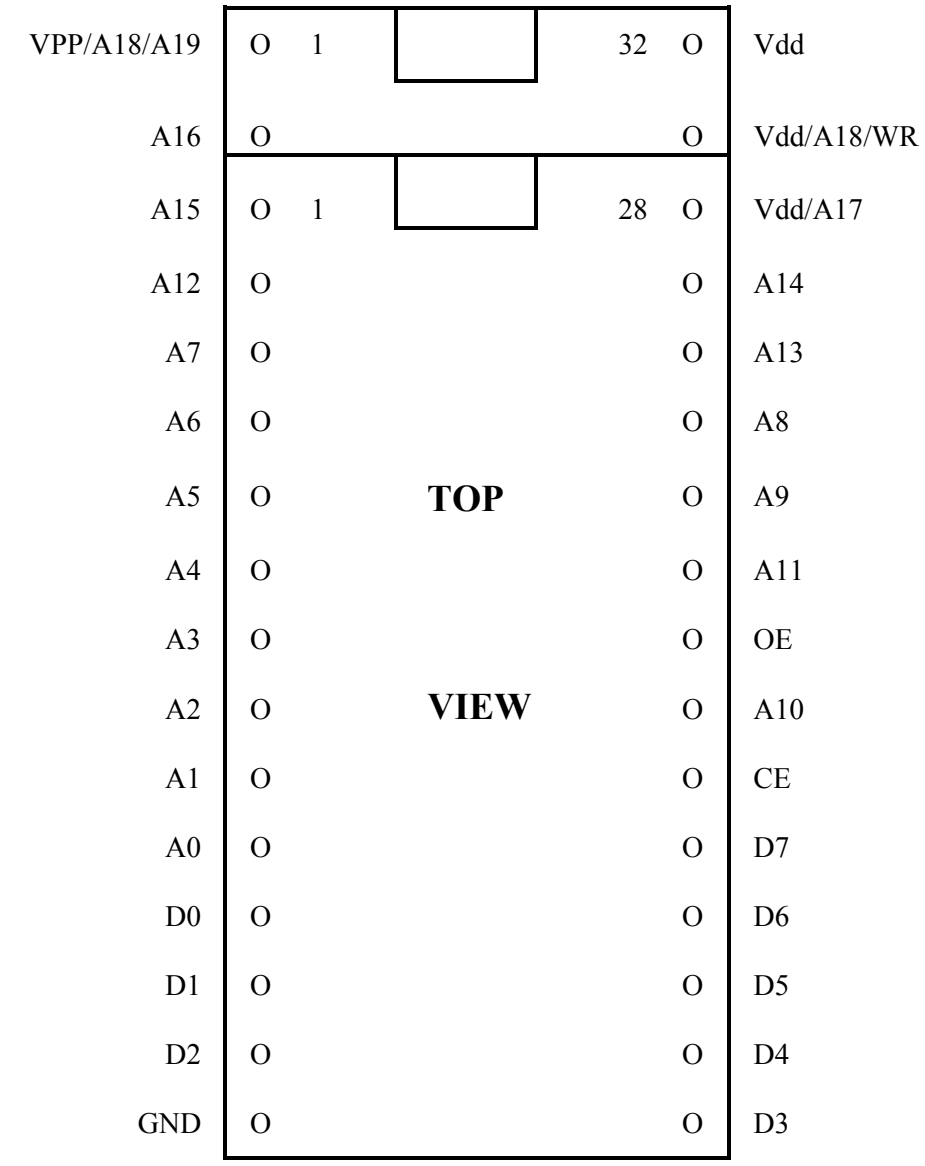
BTMD	Function	BTSZ
Pin 3-5	CS0 connected to 8 bit socket	ISP-Pin 9-10
Pin 4-6	CS1 connected to 64 bit Flash	ISP-Pin 9-10
Pin 3-4	CS0 connected to 64 bit Flash	open
Pin 5-6	CS1 connected to 8 bit socket	open

Pinout of wrap connector ISP:



Please check for correct pin compatibility before mounting any device. 28 pin and 32 pin packages must be inserted into socket as shown below only during power down. Any insertion of other types or not as directed may cause permanent damage to the device and/or the board.

Socket Pinout:



Note! Only <u>3.3 volt</u> devices are supported!

6.2.4 The Static RAM Area

The CPC45 contains a static ram area consisting of 4 SRAM devices with either 128Kx8 or 512Kx8 capacity, which allows for a total capacity of 512KByte or 2MByte at a 32 bit wide data bus. The SRAM is located on the local PCI bus of the MPC8245 controlled by the PCI9030 I/O accelerator chip via its CS0 select line. The access address as well as all access parameters can be adjusted within the PCI9030.

The SRAM bank is controlled via the PCI9030 according to the following table:

SRAM Bank	PCI9030	Description
A0-A16	LA2-LA18	address
A17/Vcc	VCB/LA19	via link SRS
A18	LA20	address
WR	LWR0-LWR3	via ispLSI
CE	CS0	via MAX793
OE	LRD	output enable
D0-D31	LD0-LD31	data path

The contents of the SRAM area is protected against data loss by a backup circuitry. The backup power is supplied by a service free gold capacitor. An extended backup time can be reached, if the **non Compact PCI conforming** standby line on ST1 pin d25 is used to supply the necessary backup power. In any case, the backup time mainly depends on the used SRAM devices and their standby power consumption. The backup feature of the CPC45 cannot be disabled. The backup power is supplied to the SRAM area as well as to the onboard real time clock.

6.3 The Serial I/O-Interface

6.3.1 The ST16C2550 Dual UART

The CPC45 contains a ST16C2550 Dual UART device. The UART supports two I/O channels with a 16 byte receive and a 16 byte transmit FIFO. The UART is located on the local PCI bus of the MPC8245 controlled by the PCI9030 PCI I/O accelerator chip via its CS1 and CS2 select lines as two 8 bit devices. The access address as well as all access parameters can be adjusted within the PCI9030. The UART offers two interrupt lines connected to the MPC8245 IRQ0 line if the according enable bits within the (I)nterrupt (E)nable (R)egister (2) at location PCI9030-CS3+$02 are set. The status of these interrupt lines is reflected within the (I)nterrupt (S)tatus (R)egister (2) at location PCI9030-CS3+$03 independent of the enable bit state. The UART device is supplied with an external clock of 7.3728MHz which allows for data rates up to 460.8Kbps.

Channel I is accessible through an I/O module via a 9 pin DSUB connector on the frontpanel. The I/O-Lines of channel II are TTL compatible, 5 volt tolerant, and accessible via the 8 pin wrap connector ST8. The desired EIA interface standard of both ports can be individually realised by two I/O modules of various types. connector on the frontpanel

UART channel A:

address	read mode		write mode	
CS1+$0	receive holding register	RHR	THR	transmit holding register
CS1+$1			IER	interrupt enable register
CS1+$2	interrupt status register	ISR	FCR	FIFO control register
CS1+$3			LCR	line control register
CS1+$4			MCR	modem control register
CS1+$5	line status register	LSR		
CS1+$6	modem status register	MSR		
CS1+$7	scratchpad register	SPR	SPR	scratchpad register

UART channel B:

address	read mode		write mode	
CS2+$0	receive holding register	RHR	THR	transmit holding register
CS2+$1			IER	interrupt enable register
CS2+$2	interrupt status register	ISR	FCR	FIFO control register
CS2+$3			LCR	line control register
CS2+$4			MCR	modem control register
CS2+$5	line status register	LSR		
CS2+$6	modem status register	MSR		
CS2+$7	scratchpad register	SPR	SPR	scratchpad register

Bit map of the (I)nterrupt (E)nable (R)egister (2):

IER2 @ $02	D7	D6	D5	D4	D3	D2	**D1**	**D0**
read/write	ABO	KEY1	KEY2	RTC	SMN	DEG	**SIO2**	**SIO1**
reset state	0	0	0	0	0	0	**0**	**0**
SIO 1 IRQ disabled	x	x	x	x	x	x	**x**	**0**
SIO 1 IRQ enabled	x	x	x	x	x	x	**x**	**1**
SIO 2 IRQ disabled	x	x	x	x	x	x	**0**	**x**
SIO 2 IRQ enabled	x	x	x	x	x	x	**1**	**x**

Bit map of the (I)nterrupt (S)tatus (R)egister (2):

ISR2 @ $03	D7	D6	D5	D4	D3	D2	**D1**	**D0**
read only	ABO	KEY1	KEY2	RTC	SMN	DEG	**SIO2**	**SIO1**
SIO 1 IRQ not active	x	x	x	x	x	x	**x**	**0**
SIO 1 IRQ active	x	x	x	x	x	x	**x**	**1**
SIO 2 IRQ not active	x	x	x	x	x	x	**0**	**x**
SIO 2 IRQ active	x	x	x	x	x	x	**1**	**x**

For detailed programming information and chip description, please refer to ST16C2550 Data Sheet !

6.3.2 The EIA Module Socket

The CPC45 offers a 22 pin socket for various types of I/O modules. The module connects the UART I/O signals to the 9 pin DSUB frontpanel connector ST7 according to following table. The signals leading to the UART device are 5 volt tolerant.

UART-1	Module Pin
VCC	2
GND	22
DTR	8
CTS	10
TXD	12
RTS	14
RXD	16
DSR	18
DCD	20

Module Pin	DSUB	EIA-RS422
	6	VCC
3	5	GND
7	3	TXD+
9		
11	8	TXD
13		
15	9	RXD-
17		
19	4	RXD+

6.3.3 The EIA Warp Connector

The 10 pin wrap connector ST8 contains the following 5 volt tolerant TTL signals. It can be used for an external EIA transceiver.

UART-2	Wrap Pin
GND	1
TXD	3
DTR	5
n.c.	7
DCD	9

Wrap Pin	UART-2
2	VCC
4	RXD
6	RTS
8	CTS
10	GND

(n.c. no connection)

6.4 The I²C Bus

The I²C bus onboard the CPC45 is controlled via the SDA and SCL pins of the MPC8245 and contains a real-time clock, an EEPROM and a system hardware monitor device.

6.4.1 The EEPROM

The CPC45 offers a 16KBit serial EEPROM for storing system or board parameters. The 24C164 device is internally organised to 2048 x 8 bit and allows for at least 100000 write cycles with a typical cycle time of 5ms.

The 24C164 device responds on the I²C bus within the address range from $B0 up to $BF.

For detailed programming information and chip description, please refer to 24C164 Data Sheet !

6.4.2 The SODIMM SPD Feature

The SODIMM modules offer usually a serial EEPROM for module parameters. The specifications of the mounted device must be taken out of the data sheet of the used RAM module. If the access address leads to a double addressing with any other device on the I²C bus, it can be disconnected by the SMD link R91. The used SODIMM (S)erial (P)resence (D)etect device responds at $A0 and $A1 for memory transactions. The access addresses $60 and $61 refer to the SPD protection register.

For detailed programming information and chip description, please refer to SODIMM Data Sheet !

For SPD support, please refer to software documentation !
There is no SPD support in boot code at the moment !

6.4.3 The Real Time Clock

The PCF8563 RTC features a clock function with a calendar and an universal timer with alarm and interrupt function. The RTC is protected against data loss by a backup circuitry. The backup feature, supplied from a service free gold capacitor, cannot be disabled. For long time applications a non Compact PCI compliant standby line on ST1 pin d25 can be used to supply the necessary backup power. The maskable interrupt can be generated on the MPC8245 **IRQ line 0** if the according enable bit within the IER2 at location PCI9030-CS3+$02 is set to high. The IER2 contents is cleared after reset and can be read back for verification. The current status of the RTC interrupt line can be detected within the ISR2 register at location PCI9030-CS3+$03.

The RTC device responds on the I^2C bus at address $A3 for read and $A2 for write accesses.

Bit map of the (I)nterrupt (E)nable (R)egister (2):

IER2 @ $02	D7	D6	D5	**D4**	D3	D2	D1	D0
read/write	ABO	KEY1	KEY2	**RTC**	SMN	DEG	SIO2	SIO1
reset state	0	0	0	**0**	0	0	0	0
RTC IRQ disabled	x	x	x	**0**	x	x	x	x
RTC IRQ enabled	x	x	x	**1**	x	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (2):

ISR2 @ $03	D7	D6	D5	**D4**	D3	D2	D1	D0
read only	ABO	KEY1	KEY2	**RTC**	SMN	DEG	SIO2	SIO1
RTC IRQ not active	x	x	x	**0**	x	x	x	x
RTC IRQ active	x	x	x	**1**	x	x	x	x

6.4.3.1 The PCF8563T Address Map

Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
$00	Control/Satus 1	TEST1	0	STOP	0	TESTC	0	0	0
$01	Control/Status 2	0	0	0	TI/TP	AF	TF	AIE	TIE
$0D	CLKOUT frequency	FE	--	--	--	--	--	FD1	FD0
$0E	Timer control	TE	--	--	--	--	--	TD1	TD0
$0F	Timer countdown value	<timer countdown value>							
Address	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
		BCD format tens nibble				BCD format units nibble			
$02	Seconds	VL	<seconds 00 to 59 coded in BCD>						
$03	Minutes	--	<minutes 00 to 59 coded in BCD>						
$04	Hours	--	--	<hours 00 to 23 coded in BCD>					
$05	Days	--	--	<days 01 to 31 coded in BCD>					
$06	Weekdays	--	--	--	--	--	<weekday 0 to 6>		
$07	Month/Century	C	--	--	<month 01 to 12 coded in BCD>				
$08	Years	<years 00 to 99 coded in BCD>							
$09	Minute alarm	AE	<minute alarm 00 to 59 coded in BCD>						
$0A	Hour alarm	AE	--	<hour alarm 00 to 23 coded in BCD>					
$0B	Day alarm	AE	--	<day alarm 01 to 31 coded in BCD>					
$0C	Weekday alarm	AE	--	--	--	--	<weekday alarm 0 to 6>		

For detailed programming information and chip description, please refer to Philips PCF8563 Data Sheet !

6.4.4 The System Hardware Monitor

The board ambient and supply conditions of the CPC45 can be sensed by the microprocessor system hardware monitor LM81. It offers the monitoring of the board ambient temperature, all board supply voltages, the onboard battery condition and the voltage range of an external battery. It is able to generate a hard reset to the onboard CPU, caused by a programmable threshold voltage. The VID0-4 inputs are used to monitor a 5 bit hardware revision of the board. A maskable interrupt can be generated on the MPC8245 **IRQ line 0** if the according enable bit within the IER2 at location PCI9030-CS3+$02 is set to high. The IER2 contents is cleared after reset and can be read back for verification. The current status of the LM81 interrupt line can be detected within the ISR2 register at location PCI9030-CS3+$03.

The LM81 device responds on the I^2C bus at address $59 for read and $58 for write accesses.

Bit map of the (I)nterrupt (E)nable (R)egister (2):

IER2 @ $02	D7	D6	D5	D4	**D3**	D2	D1	D0
read/write	ABO	KEY1	KEY2	RTC	**SMN**	DEG	SIO2	SIO1
reset state	0	0	0	0	**0**	0	0	0
LM81 IRQ disabled	x	x	x	x	**0**	x	x	x
LM81 IRQ enabled	x	x	x	x	**1**	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (2):

ISR2 @ $03	D7	D6	D5	D4	**D3**	D2	D1	D0
read only	ABO	KEY1	KEY2	RTC	**SMN**	DEG	SIO2	SIO1
LM81 IRQ not active	x	x	x	x	**0**	x	x	x
LM81 IRQ active	x	x	x	x	**1**	x	x	x

VID0 – VID4 Hardware Revision Code

LM81 VIDx Pins	VID3	VID3	VID2	VID1	VID0
	Flash Type	Rev. Bit 3	Rev. Bit 2	Rev. Bit 1	Rev. Bit 0
RC28F160**F**3T Flashes mounted	0	0	1	0	0
RC28F160**C**3T Flashes mounted	1	0	1	0	0

The pins of the LM81 are connected according to following table.

connected to:	LM81		connected to:
pulldown to ground	A0/NTO	VID0	ID0 (R22 inserted == 0)
pulldown to ground	A1	VID1	ID1 (R23 inserted == 0)
CPU-SDA	SMBdata	VID2	ID2 (R24 not inserted == 1)
CPU-SCL	SMBclock	VID3	ID3 (R25 inserted == 0)
not used and left open	FAN1	VID4	ID4 (R26 inserted == 0 for 28F160**F**) ID4 (R26 not inserted == 1 for 28F160**C**)
not used and left open	FAN2	Vccp1	-12V of CPCI bus
not used and left open	CI	+2.5Vin	VEE = CPU Core supply
not used and left open	OVTA	+3.3Vin	VDD = 3.3V for CPU & Logic
3.3V supply	V+	+5.0Vin	VCC = 5V for Logic
CPU-IRQ	INT	+12Vin	+12V of CPCI bus
not used and left open	DACO/NTI	Vccp2	standby line voltage
CPU-Reset	RESET	GND	ground

The voltage detection of the -12V supply is handled by a resistor divider against the +5V supply. The used division factor formats the -12V to +1.25V according to the formula:

R1 = 141K R2 = 40K Vcc = 5V V_{-12} = -12V

$$Vccp1 = Vcc \times \left(1 - \frac{R2}{R1+R2}\right) + V_{-12} \times \frac{R2}{R1+R2}$$

Vccp1 = 3.895V + (-12V) x 0.221 = 1.243V

For detailed programming information and chip description, please refer to LM81 Data Sheet !

6.5 Miscellaneous

6.5.1 The Backup Feature

The backup feature of the CPC45 is used to protect the **RTC** as well as the **SRAM** area. Both devices are connected to the MAX-793, which controls the backup supply and the power up and down sequences to avoid unintended write pulses. The backup power is supplied by a **service free gold capacitor**. The RTC as well as the SRAM area cannot be disconnected from the backup power.

The gold capacitor allows for a service free short time backup without any battery or other time or temperature degrading parts. If the backup time should be extended the backup power can be supplied via the non Compact PCI compliant standby line on connector ST1, pin d25. The external supply voltage should not exceed 3.9 volts and not fall below 2.5 volts to ensure correct data retention.

The power consumption table of all backup connected devices:

device:	**max. current:**	**total:**
MAX793	1µA	1µA
PCF8563	0,5µA @ 3volts	0,5µA
K6T4008V1C-B70	15µA @ 3volts	120µA

6.5.2 The Board Reset Function

The CPC45 features four independent reset controllers to detect several reset conditions. The possible reset conditions and destinations are listed in following table.

reset		reset condition		reset		
device	location	power up	others	threshold	status	signal
MAX793S	J11	yes	watchdog	2.85-3.00	BSR-D5	WRST#
MAX811S	J33	yes	manual	2.85-3.00	BSR-D4	KRST#
MAX811S	J34	yes	CPCI - FAL#	2.85-3.00	BSR-D4/D5	MRST#
LM81	J10	yes	limits	programmable	---	HRST#

The board status register contents is only cleared by a power up reset or by a the assertion of the Compact PCI FAL# line. A manual reset, a watchdog reset or a LM81 reset does not clear the board status register, i.e. the reset source can be identified by the register contents.

BSRG @ $05	**D7**	D6	**D5**	**D4**	D3	D2	D1	D0
read only	**WDGE**	---	**WRST**	**KRST**	CSW3	CSW2	CSW1	CSW0
power up reset	**0**	x	**0**	**0**	x	x	x	x
CPCI-FAL# reset	**0**	x	**0**	**0**	x	x	x	x
manual reset	**0**	x	**x**	**1**	x	x	x	x
watchdog reset	**0**	x	**1**	**x**	x	x	x	x
LM81 reset	x	x	x	x	x	x	x	x

6.5.3 The Board Control Register

The CPC45 offers a (B)oard (C)ontrol (R)e(G)ister for LED control, flash write protection and reset status clear functions. The BCRG contents is cleared after reset and it can be read back for verification.

Bit map of the (B)oard (C)ontrol (R)e(G)ister:

BCRG @ $04	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
read/write	**WRSE**	**KRSE**	**FWRE**	**FWPT**	**LED2**	**LED1**	**---**	**---**
reset state	0	0	0	0	0	0	0	0
user LED 1 on	x	x	x	x	x	1	x	x
user LED 1 off	x	x	x	x	x	0	x	x
user LED 2 on	x	x	x	x	1	x	x	x
user LED 2 off	x	x	x	x	0	x	x	x
Flash WP-pin low	x	x	x	0	x	x	x	x
Flash WP-pin high	x	x	x	1	x	x	x	x
Flash write disabled	x	x	0	x	x	x	x	x
Flash write enabled	x	x	1	x	x	x	x	x
key reset status hold	x	0	x	x	x	x	x	x
key reset status clear	x	1	x	x	x	x	x	x
watchdog reset status hold	0	x	x	x	x	x	x	x
watchdog reset status clear	1	x	x	x	x	x	x	x

6.5.4 Hardware Watchdog Timer

The CPC45 features a fixed rate hardware timer for watchdog purposes, which can be enabled by software. Once enabled, it only can be disabled by a hardware reset or a special command sequence. The time out rate is set to about 1.6 seconds. Within that time at least one read access must be performed to the (W)atchdog (R)etrigger (R)egister, located at the PCI9030-CS3+$06, to retrigger the timer.
In case a reset has been issued by the watchdog timer, the WDGE bit within the (B)oard (S)tatus (R)e(G)ister is cleared, the watchdog is disabled and the WRST bit is set.
The watchdog is started by any command to the address location PCI9030-CS3+$06. It can be stopped by two sequential byte write commands to the same location with the data contents of $55 and $AA.

Bit map of the (B)oard (S)tatus (R)e(G)ister:

BSRG @ $05	**D7**	D6	**D5**	D4	D3	D2	D1	D0
read/write	**WDGE**	---	**WRST**	KRST	CSW3	CSW2	CSW1	CSW0
power up reset	**0**	0	**0**	0	x	x	x	x
watchdog caused reset	**x**	x	**1**	x	x	x	x	x
watchdog disabled	**0**	x	**x**	x	x	x	x	x
watchdog enabled	**1**	x	**x**	x	x	x	x	x

Bit map of the (W)atchdog (R)etrigger (R)e(G)ister:

WRRG @ $06	D7	D6	D5	D4	D3	D2	D1	D0
start watchdog	any write command							
prestop watchdog	0	1	0	1	0	1	0	1
stop watchdog	1	0	1	0	1	0	1	0

6.6 Board Identification

6.6.1 ispLSI Revision Register 1

For software adoption, the CPC45 contains a (P)lsi (R)evision (R)egister (1), which can be read out at location PCI9030-CS3+$08.

Bit map of the (P)lsi (R)evision (R)egister (1):

PRR1 @ $08	D7	D6	D5	D4	D3	D2	D1	D0
ispLSI Revision 1	0	0	0	0	0	0	0	1

6.6.2 ispLSI Revision Register 2

For software adoption, the CPC45 contains a (P)lsi(R)evision (R)egister (2), which can be read out at location PCI9030-CS3+$09.

Bit map of the (P)lsi (R)evision (R)egister (2):

PRR2 @ $09	D7	D6	D5	D4	D3	D2	D1	D0
ispLSI Revision 2	0	0	0	0	0	1	0	0

The ispLSI content can be identified by a number with 7 digits labelled on the device. The 4 LSB digits are reflected in the ispLSI Revision Register 1 + 2.

The register content shown above is for ispLSI version 2860104!

6.6.3 Hardware Revision ID

The hardware revision (PCB) is reflected by the VID0-3 bits of the monitor chip LM81 VID/Fan division register (offset 0x48). The VID4 bit in the VID4 register (offset 0x49) is set to 0 for RC28F160F3T Flash devices and set to 1 for RC28F160C3T Flashes used .
See also LM81 description in chapter 6.4.4.

Register	Address	Reset Value							
VID/Fan division	0x48	0	1	0	1	0	1	0	0
VID4	0x49	1	0	0	0	0	0	0	x

6.7 The Local PCI Bus

The CPC45 contains several PCI devices, located on the local PCI bus. The CompactPCI side is buffered via the transparent PCI-to-PCI bridge 21150 from Intel. The devices on the local PCI bus can be detected by configuration cycles according to following table.

local PCI controlled devices	ID-Select	Size	Type
MPC8245	AD12	32Bit	master/slave
PCI9030 I/O Accelerator	AD13	32Bit	slave only
D6729 CF-Card Controller	AD14	32Bit	slave only
LAN I82259 Ethernet Controller	AD15	32Bit	master/slave
SB21150AC PCI to PCI Bridge	AD16	32Bit	master/slave

The local PCI device interrupt structure

local PCI device	device interrupt line	MPC8245 destination
PCI9030	INTA	not connected
PD6729	PCI_IRQ3/INTA	IRQ1
I82259	INTA	IRQ2
PCI21150	no IRQ line	---

6.7.1 The PCI9030 I/O Accelerator

The CPC45 uses the PCI9030 I/O Accelerator from PLX to adapt several peripheral devices. The SRAM area, the DUART, the 8 digit display and the ispLSI contained register set are controlled by the PCI9030 in 8 and 32 bit **non multiplexed** bus mode. The PCI9030 responds to configuration cycles on the local PCI bus at address **AD13** high. The hot swap control pins are not used and left open or pulled to high. The interrupt pin of the PCI9030 is not used. The pins of the PCI9030 are used according to following table.

pin	name	function	destination	description	data bus	address bus
147	CS0	used	SRAM	select line	LD(0-31)	LA(2-20)
148	CS1	used	SIO-A	select line	LD(0-7)	LA(0-2)
156	CS2/GPIO2	CS2 used	SIO-B	select line	LD(0-7)	LA(0-2)
157	CS3/GPIO3	CS3 used	ispLSI	select line	LD(0-7)	LA(0-6)
137	LA27/GPIO4	not used	pull up			
136	LA25/GPIO6	not used	pull up			
135	LA26/GPIO5	not used	pull up			
134	LA24/GPIO7	not used	pull up			
94	GPIO8	not used	pull up			
154	WAIT/GPIO0	not used	pull up			
155	LLOCK/GPIO1	not used	pull up			
153	L1INT	not used	pull down			
152	L2INT	not used	pull down			
143	READY	not used	pull up			
144	BTERM	not used	pull up			
139	BLAST	not used	pull up			
138	ADS	not used	pull up			
75	ALE	not used	pull down			
151	LREQ	not used	pull down			
158	EECS	E^2PROM	93CS66	select		
159	EEDO	E^2PROM	93CS66	data out		
161	EEDI	E^2PROM	93CS66	data in		
160	EESK	E^2PROM	93CS66	clock		
103	LPMESET	not used	pull down			
126	LPMINT	not used	pull up			
145	LCLK	clock	OSC2	60MHz		
170	INTA	interrupt	ispLSI	not used		

For detailed programming information and chip description, please refer to PLX PCI9030 Data Book !

6.7.2 The D6729 CF-Card Controller

The compact flash interface of the CPC45 is supported by the PC-Card controller PD6729 from Intel. The PD6729 responds to configuration cycles on the local PCI bus at address **AD14** high. The interrupt pin INTA of the PD6729 is routed via the ispLSI to the **IRQ1** line of the MPC8245. All other interrupt pins are not connected and left open. The PD6729 is able to handle two PCMCIA sockets, but only socket A is connected to the 50 pin CF-Card connector according to following table.

Pin assignment of the CF-Card connector ST6:

name	pin		pin	name
GND	1		26	A_CD1#
A_D3	2		27	A_D11
A_D4	3		28	A_D12
A_D5	4		29	A_D13
A_D6	5		30	A_D14
A_D7	6		31	A_D15
A_CE1#	7		32	A_CE2#
A_A10	8		33	A_VS1
A_OE#	9		34	A_IORD#
A_A9	10		35	A_IOWR#
A_A8	11		36	A_WE#
A_A7	12		37	A_RDY
VCC/VDD	13		38	VCC/VDD
A_A6	14		39	(CSEL) GND
A_A5	15		40	A_VS2
A_A4	16		41	A_RESET
A_A3	17		42	A_WAIT#
A_A2	18		43	A_INPAC#
A_A1	19		44	A_REG#
A_A0	20		45	A_BVD2
A_D0	21		46	A_BVD1
A_D1	22		47	A_D8
A_D2	23		48	A_D9
A_WP	24		49	A_D10
A_CD2#	25		50	GND

For detailed programming information and chip description, please refer to PD6729 Data Sheet !

6.7.3 LAN 82259 Ethernet Controller

The LAN interface of the CPC45 is realized by the Intel 82559 fast ethernet PCI controller. It contains a 10Base-T and 100Base-T, IEEE802.3 compatible PHY with a 32bit PCI master interface. The 82559 responds to configuration cycles on the local PCI bus at address **AD15** high. The interrupt pin INTA of the 82559 is routed via the ispLSI to the **IRQ2** line of the MPC8245.
The hot swap control pins are not used and left open or pulled to high. The test port interface is accessible via the molex connector TST. The serial EEPROM interface of the 82559 is connected to a 93C46 device. All other memory control lines are left open. The LED interface handles a speed LED and a link integrity controlled activity LED. The pins of the 82559 are used according to following table.

pad	name	function	destination	description
P9	CLK25/FLA16	not used	open	
M10	EESK/FLA15	EESK	EEPROM	NM93CS46
N10	EEDO/FLA14	EEDO	EEPROM	NM93CS46
P10	EEDI/FLA13	EEDI	EEPROM	NM93CS46
M11	MCNTSM/FLA12	not used	open	
M12	MINT/FLA11	not used	open	
N13	MRING/FLA10	not used	open	
P13	MRST/FLA9	not used	open	
N14	IOCHRDY/FLA8	not used	open	
M13	CLKEN/FLA7	not used	open	
M14...	FLA6-FLA2	not used	open	
J12	AUXPWR/FLA1	AUXPWR	pull down	
J13	PCIMODE/FLA0	not used	open	
J14...	FLD7-FLD0	not used	open	
P7	EECS	used	EEPROM	NM93CS46
N9	AEN/FLCS	not used	open	
M8	FLOE	not used	open	
M9	FLWE	not used	open	
L7	CFCS	not used	open	
L8	CFCLK	not used	open	
B10	SMBALRT		pull up	
A10	SMBCLK		I^2C-SCL	
C9	SMBD		I^2C-SDA	
A13	TEST	TAP	TST-Pin 1	pull down
D13	TEXEC	TAP	TST-Pin 3	exec.enable
D14	TCK	TAP	TST-Pin 4	test clock
D12	TDI	TAP	TST-Pin 5	data in
B12	TDO	TAP	TST-Pin 6	data out

For detailed programming information and chip description, please refer to Intel 82559 Data Sheet!

6.7.4 SB21150AC PCI to PCI Bridge

The CompactPCI interface of the CPC45 is realised via the transparent PCI-to-PCI bridge SB21150AC from Intel. The 21150 responds to configuration cycles on the local PCI bus at address **AD16** high. The primary bus handles the local PCI bus onboard the CPC45, while the secondary bus side of the 21150 controls the CompactPCI system slot functions. The GPIO(0-3) lines are not used for any purpose and tied to high by pull-up resistors. The clock driver ports from CLKOUT0 to CLKOUT7 are used. CLOCKOUT 8 & 9 are not connected. Both bus sides run always in 33MHz mode, i.e. the M66ENA and CONFIG66 pins on the primary side are tied to logical low. All hotswap control lines are not used and left open. The pins of the 21150 are used according to following table.

pad	name	function	destination
29	CLKOUT0	reference clock	21150-CLK input
30	CLKOUT1	clock	CompacPCI J1
32	CLKOUT2	clock	CompacPCI J1
33	CLKOUT3	clock	CompacPCI J1
35	CLKOUT4	clock	CompacPCI J1
36	CLKOUT5	clock	CompacPCI J1
38	CLKOUT6	clock	CompacPCI J1
39	CLKOUT7	clock	CompacPCI J1
41	CLKOUT8	not used	open
42	CLKOUT9	not used	open
28	GPIO0	not used	pull up
27	GPIO1	not used	pull up
25	GPIO2	not used	pull up
24	GPIO3	not used	pull up
125	CONFIG66	33MHz mode	pull down
153	S_M66ENA	low	CompacPCI J1
102	S_M66ENA	low	pull down

For detailed programming information and chip description, please refer to Intel 21150 Data Sheet!

6.7.5 The CompactPCI Connector Pin assignment J1 / J2

Pin	F	E	D	C	B	A	Z
J1-1	GND	VCC	+12V	TRST#	-12V	VCC	GND
J1-2	GND	TDI	TDO	TMS	VCC	TCK	GND
J1-3	GND	INTD#	VCC	INTC#	INTB#	INTA#	GND
J1-4	GND	INTS	INTP	VIO	HLTY	reserved	GND
J1-5	GND	GNT#	GND	RST#	reserved	reserved	GND
J1-6	GND	AD[31]	CLK	VDD	GND	REQ#	GND
J1-7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]	GND
J1-8	GND	AD[24]	AD[25]	VIO	GND	AD[26]	GND
J1-9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#	GND
J1-10	GND	AD[19]	AD[20]	VDD	GND	AD[21]	GND
J1-11	GND	C/BE[2#]	GND	AD[16]	AD[17]	AD[18]	GND
J1-12	K e y						
J1-13	K e y						
J1-14	K e y						
J1-15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	VDD	GND
J1-16	GND	LOCK#	STOP#	VIO	GND	DEVSEL#	GND
J1-17	GND	PERR#	GND	SBO#	SDONE	VDD	GND
J1-18	GND	C/BE[1]#	PAR	VDD	GND	SERR#	GND
J1-19	GND	AD[13]	GND	AD[14]	AD[15]	VDD	GND
J1-20	GND	AD[10]	AD[11]	VIO	GND	AD[12]	GND
J1-21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	VDD	GND
J1-22	GND	AD[5]	AD[6]	VDD	GND	AD[7]	GND
J1-23	GND	AD[2]	VCC	AD[3]	AD[4]	VDD	GND
J1-24	GND	ACK64#	AD[0]	VIO	VCC	AD[1]	GND
J1-25	GND	VCC	VDD	ENUM#	REQ64#	VCC	GND
J2-1	GND	REQ2#	GNT1#	REQ1#	GND	CLK1	GND
J2-2	GND	REQ3#	GNT2#	SYSEN#	CLK3	CLK2	GND
J2-3	GND	GNT4#	REQ4#	GNT3#	GND	CLK4	GND
J2-4	GND	C/BE[6]#	GND	C/BE[7]#	reserved	VIO	GND
J2-5	GND	PAR64	C/BE[4]#	VIO	GND	C/BE[5]#	GND
J2-6	GND	AD[60]	GND	AD[61]	AD[62]	AD[63]	GND
J2-7	GND	AD[57]	AD[58]	VIO	GND	AD[59]	GND
J2-8	GND	AD[53]	GND	AD[54]	AD[55]	AD[56]	GND
J2-9	GND	AD[50]	AD[51]	VIO	GND	AD[52]	GND
J2-10	GND	AD[46]	GND	AD[47]	AD[48]	AD[49]	GND
J2-11	GND	AD[43]	AD[44]	VIO	GND	AD[45]	GND
J2-12	GND	AD[39]	GND	AD[40]	AD[41]	AD[42]	GND
J2-13	GND	AD[36]	AD[37]	VIO	GND	AD[38]	GND
J2-14	GND	AD[32]	GND	AD[33]	AD[34]	AD[35]	GND
J2-15	GND	GNT5#	REQ5#	FAL#	GND	reserved	GND
J2-16	GND	reserved	GND	DEG#	reserved	reserved	GND
J2-17	GND	GNT6#	REQ6#	PRST#	GND	reserved	GND
J2-18	GND	reserved	GND	reserved	reserved	reserved	GND
J2-19	GND	RSV	RSV	RSV	GND	GND	GND
J2-20	GND	RSV	GND	RSV	GND	CLK5	GND
J2-21	GND	RSV	RSV	RSV	GND	CLK6	GND
J2-22	GND	GA0	GA1	GA2	GA3	GA4	GND
Pin	**F**	**E**	**D**	**C**	**B**	**A**	**Z**

7. Interrupt Structure

7.1 The Interrupt Structure

The CPC45 contains 10 local interrupt sources and 5 possible offboard sources. Each interrupt source has an individual mask bit and a real state status register bit. The interrupt priorisation of all interrupt sources can be freely handled according to the users' demands by software.

Each interrupt source can be enabled or disabled within the (I)nterrupt (E)nable (R)egister (1) and (2) at the PCI9030 locations CS3+$00 and CS3+$02. The contents of the IER1 and IER2 is cleared after reset and can be read back for verification. The current state of each interrupt source can be checked within the (I)nterrupt (S)tatus (R)egister (1) and (2) at the PCI9030 locations CS3+$01 and CS3+$03. The status of each interrupt line is valid at any time, no matter if the according interrupt line is enabled or not.

Attention !

The interrupt signals INTA to INTD refer to the CompactPCI bus only !
The local PCI bus does not contain any of these INTA to INTD signals !

The local PCI device interrupts are fixed to certain CPU interrupt lines. Any modification of the default interrupt distribution must be factory arranged within the CTL-ispLSI.

The interrupt structure of the MPC8245 is realised according to following table.

MPC8245	External Source
IRQ0	SIO-A / SIO-B / Abort Key / Key I / Key II / RTC / LM81
IRQ1	PCMCIA
IRQ2	Ethernet
IRQ3	Compact PCI : INTA / INTB / INTC / INTD
IRQ4	not used yet

The local PCI device interrupt lines are used

local PCI device	device interrupt line	MPC8245 destination
PCI9030	INTA	not connected
PD6729	PCI_IRQ3/INTA	IRQ1
I82259	INTA	IRQ2
PCI21150	no IRQ line	---

Bit map of the (I)nterrupt (E)nable (R)egister (1):

IER1 @ $00	D7	D6	D5	D4	D3	D2	D1	D0
read/write	IERA	IERB	IERC	IERD	---	---	---	---
reset state	0	0	0	0	0	0	0	0
CPCI-INTD disabled	x	x	x	0	x	x	x	x
CPCI-INTD enabled	x	x	x	1	x	x	x	x
CPCI-INTC disabled	x	x	0	x	x	x	x	x
CPCI-INTC enabled	x	x	1	x	x	x	x	x
CPCI-INTB disabled	x	0	x	x	x	x	x	x
CPCI-INTB enabled	x	1	x	x	x	x	x	x
CPCI-INTA disabled	0	x	x	x	x	x	x	x
CPCI-INTA enabled	1	x	x	x	x	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (1):

ISR1 @ $01	D7	D6	D5	D4	D3	D2	D1	D0
read only	IERA	IERB	IERC	IERD	0	0	0	0
CPCI-INTD inactive	x	x	x	0	x	x	x	x
CPCI-INTD active	x	x	x	1	x	x	x	x
CPCI-INTC inactive	x	x	0	x	x	x	x	x
CPCI-INTC active	x	x	1	x	x	x	x	x
CPCI-INTB inactive	x	0	x	x	x	x	x	x
CPCI-INTB active	x	1	x	x	x	x	x	x
CPCI-INTA inactive	0	x	x	x	x	x	x	x
CPCI-INTA active	1	x	x	x	x	x	x	x

Bit map of the (I)nterrupt (E)nable (R)egister (2):

IER2 @ $02	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABO	KY1	KY2	RTC	SMN	DEG	SIO2	SIO1
reset state	0	0	0	0	0	0	0	0
SIO1 IRQ disabled	x	x	x	x	x	x	x	0
SIO1 IRQ enabled	x	x	x	x	x	x	x	1
SIO2 IRQ disabled	x	x	x	x	x	x	0	x
SIO2 IRQ enabled	x	x	x	x	x	x	1	x
CPCI-DEG IRQ disabled	x	x	x	x	x	0	x	x
CPCI-DEG IRQ enabled	x	x	x	x	x	1	x	x
LM81 IRQ disabled	x	x	x	x	0	x	x	x
LM81 IRQ enabled	x	x	x	x	1	x	x	x
RTC IRQ disabled	x	x	x	0	x	x	x	x
RTC IRQ enabled	x	x	x	1	x	x	x	x
Key-2 IRQ disabled	x	x	0	x	x	x	x	x
Key-2 IRQ enabled	x	x	1	x	x	x	x	x
Key-1 IRQ disabled	x	0	x	x	x	x	x	x
Key-1 IRQ enabled	x	1	x	x	x	x	x	x
ABO-Key IRQ disabled	0	x	x	x	x	x	x	x
ABO-Key IRQ enabled	1	x	x	x	x	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (2):

ISR2 @ $03	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	KY1	KY2	RTC	SMN	DEG	SIO2	SIO1
SIO1 IRQ inactive	x	x	x	x	x	x	x	0
SIO1 IRQ active	x	x	x	x	x	x	x	1
SIO2 IRQ inactive	x	x	x	x	x	x	0	x
SIO2 IRQ active	x	x	x	x	x	x	1	x
CPCI-DEG line inactive	x	x	x	x	x	0	x	x
CPCI-DEG line active	x	x	x	x	x	1	x	x
LM81 IRQ inactive	x	x	x	x	0	x	x	x
LM81 IRQ active	x	x	x	x	1	x	x	x
RTC IRQ inactive	x	x	x	0	x	x	x	x
RTC IRQ active	x	x	x	1	x	x	x	x
Key-2 IRQ inactive	x	x	0	x	x	x	x	x
Key-2 IRQ active	x	x	1	x	x	x	x	x
Key-1 IRQ inactive	x	0	x	x	x	x	x	x
Key-1 IRQ active	x	1	x	x	x	x	x	x
ABO-Key IRQ inactive	0	x	x	x	x	x	x	x
ABO-Key IRQ active	1	x	x	x	x	x	x	x

8. Register Overview

Bit map of the (I)nterrupt (E)nable (R)egister (1):

IER1 @ $00	D7	D6	D5	D4	D3	D2	D1	D0
read/write	IERA	IERB	IERC	IERD	---	---	---	---
reset state	0	0	0	0	0	0	0	0
CPCI-INTD disabled	x	x	x	0	x	x	x	x
CPCI-INTD enabled	x	x	x	1	x	x	x	x
CPCI-INTC disabled	x	x	0	x	x	x	x	x
CPCI-INTC enabled	x	x	1	x	x	x	x	x
CPCI-INTB disabled	x	0	x	x	x	x	x	x
CPCI-INTB enabled	x	1	x	x	x	x	x	x
CPCI-INTA disabled	0	x	x	x	x	x	x	x
CPCI-INTA enabled	1	x	x	x	x	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (1):

ISR1 @ $01	D7	D6	D5	D4	D3	D2	D1	D0
read only	IERA	IERB	IERC	IERD	0	0	0	0
CPCI-INTD inactive	x	x	x	0	x	x	x	x
CPCI-INTD active	x	x	x	1	x	x	x	x
CPCI-INTC inactive	x	x	0	x	x	x	x	x
CPCI-INTC active	x	x	1	x	x	x	x	x
CPCI-INTB inactive	x	0	x	x	x	x	x	x
CPCI-INTB active	x	1	x	x	x	x	x	x
CPCI-INTA inactive	0	x	x	x	x	x	x	x
CPCI-INTA active	1	x	x	x	x	x	x	x

Bit map of the (I)nterrupt (E)nable (R)egister (2):

IER2 @ $02	D7	D6	D5	D4	D3	D2	D1	D0
read/write	ABO	KY1	KY2	RTC	SMN	DEG	SIO2	SIO1
reset state	0	0	0	0	0	0	0	0
SIO1 IRQ disabled	x	x	x	x	x	x	x	0
SIO1 IRQ enabled	x	x	x	x	x	x	x	1
SIO2 IRQ disabled	x	x	x	x	x	x	0	x
SIO2 IRQ enabled	x	x	x	x	x	x	1	x
CPCI-DEG IRQ disabled	x	x	x	x	x	0	x	x
CPCI-DEG IRQ enabled	x	x	x	x	x	1	x	x
LM81 IRQ disabled	x	x	x	x	0	x	x	x
LM81 IRQ enabled	x	x	x	x	1	x	x	x
RTC IRQ disabled	x	x	x	0	x	x	x	x
RTC IRQ enabled	x	x	x	1	x	x	x	x
Key-2 IRQ disabled	x	x	0	x	x	x	x	x
Key-2 IRQ enabled	x	x	1	x	x	x	x	x
Key-1 IRQ disabled	x	0	x	x	x	x	x	x
Key-1 IRQ enabled	x	1	x	x	x	x	x	x
ABO-Key IRQ disabled	0	x	x	x	x	x	x	x
ABO-Key IRQ enabled	1	x	x	x	x	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (2):

ISR2 @ $03	D7	D6	D5	D4	D3	D2	D1	D0
read only	ABO	KY1	KY2	RTC	SMN	DEG	SIO2	SIO1
SIO1 IRQ inactive	x	x	x	x	x	x	x	0
SIO1 IRQ active	x	x	x	x	x	x	x	1
SIO2 IRQ inactive	x	x	x	x	x	x	0	x
SIO2 IRQ active	x	x	x	x	x	x	1	x
CPCI-DEG line inactive	x	x	x	x	x	0	x	x
CPCI-DEG line active	x	x	x	x	x	1	x	x
LM81 IRQ inactive	x	x	x	x	0	x	x	x
LM81 IRQ active	x	x	x	x	1	x	x	x
RTC IRQ inactive	x	x	x	0	x	x	x	x
RTC IRQ active	x	x	x	1	x	x	x	x
Key-2 IRQ inactive	x	x	0	x	x	x	x	x
Key-2 IRQ active	x	x	1	x	x	x	x	x
Key-1 IRQ inactive	x	0	x	x	x	x	x	x
Key-1 IRQ active	x	1	x	x	x	x	x	x
ABO-Key IRQ inactive	0	x	x	x	x	x	x	x
ABO-Key IRQ active	1	x	x	x	x	x	x	x

Bit map of the (B)oard (C)ontrol (R)e(G)ister:

BCRG @ $04	D7	D6	D5	D4	D3	D2	D1	D0
read/write	WRSE	KRSE	FWRE	FWPT	LED2	LED1	---	---
reset state	0	0	0	0	0	0	0	0
user LED 1 on	x	x	x	x	x	1	x	x
user LED 1 off	x	x	x	x	x	0	x	x
user LED 2 on	x	x	x	x	1	x	x	x
user LED 2 off	x	x	x	x	0	x	x	x
Flash WP-pin low	x	x	x	0	x	x	x	x
Flash WP-pin high	x	x	x	1	x	x	x	x
Flash write disabled	x	x	0	x	x	x	x	x
Flash write enabled	x	x	1	x	x	x	x	x
key reset status hold	x	0	x	x	x	x	x	x
key reset status clear	x	1	x	x	x	x	x	x
watchdog reset status hold	0	x	x	x	x	x	x	x
watchdog reset status clear	1	x	x	x	x	x	x	x

Bit map of the (B)oard (S)tatus (R)e(G)ister:

B**SRG @ $05**	D7	D6	D5	D4	D3	D2	D1	D0
read/write	WDGE	---	WRST	KRST	CSW3	CSW2	CSW1	CSW0
power up reset	0	0	0	0	x	x	x	x
reset key caused reset	x	x	x	1	x	x	x	x
watchdog caused reset	x	x	1	x	x	x	x	x
watchdog disabled	0	x	x	x	x	x	x	x
watchdog enabled	1	x	x	x	x	x	x	x

Bit map of the (W)atchdog (R)etrigger (R)e(G)ister:

WRRG @ $06	D7	D6	D5	D4	D3	D2	D1	D0
start watchdog	any command							
prestop watchdog	1	0	1	0	1	0	1	0
stop watchdog	0	1	0	1	0	1	0	1

Bit map of the (P)lsi (R)evision (R)egister (1):

PRR1 @ $08	D7	D6	D5	D4	D3	D2	D1	D0
Revision 01	0	0	0	0	0	0	0	1

Bit map of the (P)lsi (R)evision (R)egister (2):

PRR2 @ $09	D7	D6	D5	D4	D3	D2	D1	D0
Version 04	0	0	0	0	0	1	0	0

9. Front Panel Description

9.1 Front Panel Layout

9.2 Front Panel Connectors, LEDs & Switches

The front panel of the CPC45 contains an 8 digit display, a compact flash card slot, a rotary switch and two 3-position switches, 6 LEDs, one RJ45 and two RJ11 connectors and a 9 pin DSUB connector.

Device:	Function:
Switch	Up = Reset / Down = Abort
Display	Alphanumerically 8 Digits
Switch	Up = Key I / Down = Key II
LED(gn) / LED(gn)	3.3V Power / RUN-Indicator
LED(ye) / LED(ye)	User LED 1 / User LED 2
Rotary Switch	readable 4 bit binary coded
CF-Card	ATA-Flash Card Compatible
RJ11	MPC8245-UART Channel 2 RS232 Mode
RJ11	MPC8245-UART Channel 1 RS232 Mode
DSUB-9	ST16C550 Channel 1 via I/O-Module
RJ45	Ethernet 10/100BaseT with status LEDs

9.2.1 Front Panel Connectors

Pin assignment of the DSUB, RJ45 and RJ11 connectors:

	ST7	ST3	ST4	ST5
	DSUB-9	RJ11	RJ11	RJ45
Pin:	RS422	RS232	RS232	10/100BaseT
1	---	---	---	TXD+
2	---	---	---	TXD-
3	TXD+	TXD-1	TXD-2	RXD+
4	RXD+	GND	GND	75R
5	GND	RXD-1	RXD-2	75R
6	VCC	---	---	RXD-
7	---	---	---	75R
8	TXD-	---	---	75R
9	RXD-			

Pin assignment of the CF-Card connector:

name	pin		pin	name
GND	1		26	A_CD1#
A_D3	2		27	A_D11
A_D4	3		28	A_D12
A_D5	4		29	A_D13
A_D6	5		30	A_D14
A_D7	6		31	A_D15
A_CE1#	7		32	A_CE2#
A_A10	8		33	A_VS1
A_OE#	9		34	A_IORD#
A_A9	10		35	A_IOWR#
A_A8	11		36	A_WE#
A_A7	12		37	A_RDY
VCC/VDD	13		38	VCC/VDD
A_A6	14		39	(CSEL) GND
A_A5	15		40	A_VS2
A_A4	16		41	A_RESET
A_A3	17		42	A_WAIT#
A_A2	18		43	A_INPAC#
A_A1	19		44	A_REG#
A_A0	20		45	A_BVD2
A_D0	21		46	A_BVD1
A_D1	22		47	A_D8
A_D2	23		48	A_D9
A_WP	24		49	A_D10
A_CD2#	25		50	GND

9.2.2 Front Panel LEDs

There are six LEDs on the front panel of CPC45. Two of them are integrated within the RJ45 connector of the LAN interface. The user programmable LEDs can be activated via two bits of the board control register at location PCI9030-CS3+$04.

Front panel location of the described LEDs:

power on LED	green	.	green	CPU run status LED
user programmable LED I	yellow	.	yellow	user programmable user LED II
		.		
		.		
		.	yellow	link integrity /activity LED
		.	RJ45	
		.	green	10/100 Mbit speed LED

Bit map of the (B)oard (C)ontrol (R)e(G)ister:

BCRG @ $04	D7	D6	D5	D4	**D3**	**D2**	D1	D0
read/write	WRSE	KRSE	FWRE	FWPT	**LED2**	**LED1**	---	---
reset state	0	0	0	0	**0**	**0**	0	0
user LED 1 on	x	x	x	x	**x**	**1**	x	x
user LED 1 off	x	x	x	x	**x**	**0**	x	x
user LED 2 on	x	x	x	x	**1**	**x**	x	x
user LED 2 off	x	x	x	x	**0**	**x**	x	x

9.2.3 Front Panel Switches

There are a combined reset/abort key, a double position user key and a 15 position rotary switch. The reset/abort key and the user key have three switch positions, up, center and down. The center switch position is the idle state of each switch.
The position up of the reset/abort key performs a local hardware reset to the CPC45 and the whole Compact PCI system. The position down of the reset/abort key generates a maskable interrupt to the MPC8245 on its **IRQ0** line if the according bit within the (I)nterrupt (E)nable (R)egister (2) at location PCI9030-CS3+$02 is set to high.
The user switch positions up and down generate a maskable interrupt to the MPC8245 on its **IRQ0** line if the according bit within the (I)nterrupt (E)nable (R)egister (2) at location PCI9030-CS3+$02 is set to high. The current status of the keys can be detected within the (I)nterrupt (S)tatus (R)egister (2) at location PCI9030-CS3+$03. The high active key status bit are valid at any time, no matter if the enable bit is set or not.

Bit map of the (I)nterrupt (E)nable (R)egister (2):

IER2 @ $02	**D7**	**D6**	**D5**	D4	D3	D2	D1	D0
read/write	**ABO**	**KY1**	**KY2**	RTC	SMN	DEG	SIO2	SIO1
reset state	**0**	**0**	**0**	0	0	0	0	0
Key 2 IRQ disabled	**x**	**x**	**0**	x	x	x	x	x
Key 2 IRQ enabled	**x**	**x**	**1**	x	x	x	x	x
Key 1 IRQ disabled	**x**	**0**	**x**	x	x	x	x	x
Key 1 IRQ enabled	**x**	**1**	**x**	x	x	x	x	x
ABO IRQ disabled	**0**	**x**	**x**	x	x	x	x	x
ABO IRQ enabled	**1**	**x**	**x**	x	x	x	x	x

Bit map of the (I)nterrupt (S)tatus (R)egister (2):

ISR2 @ $02	**D7**	**D6**	**D5**	D4	D3	D2	D1	D0
read only	**ABO**	**KY1**	**KY2**	RTC	SMN	DEG	SIO2	SIO1
Key 2 released	**x**	**x**	**0**	x	x	x	x	x
Key 2 pressed	**x**	**x**	**1**	x	x	x	x	x
Key 1 released	**x**	**0**	**x**	x	x	x	x	x
Key 1 pressed	**x**	**1**	**x**	x	x	x	x	x
ABO Key released	**0**	**x**	**x**	x	x	x	x	x
ABO Key pressed	**1**	**x**	**x**	x	x	x	x	x

The rotary switch has no interrupt function and its current state can be read out within the board status register at location PCI9030-CS3+$05.

Bit map of the (B)oard (S)tatus (R)e(G)ister:

BSRG @ $05	D7	D6	D5	D4	**D3**	**D2**	**D1**	**D0**
read/write	WDGE	---	WRST	KRST	**CSW3**	**CSW2**	**CSW1**	**CSW0**
power up reset	0	0	0	0	**x**	**x**	**x**	**x**
position 0	x	x	x	x	**0**	**0**	**0**	**0**
position 1	x	x	x	x	**0**	**0**	**0**	**1**
position 2	x	x	x	x	**0**	**0**	**1**	**0**
position 3	x	x	x	x	**0**	**0**	**1**	**1**
|	|	|	|	|	|	|	|	|
position D	x	x	x	x	**1**	**1**	**0**	**1**
position E	x	x	x	x	**1**	**1**	**1**	**0**
position F	x	x	x	x	**1**	**1**	**1**	**1**

10. The ispLSI & JTAG Programming Ports

The programmable logic onboard the CPC45 can be modified or updated via a PC controlled programming interface. The ISP programming port contains the necessary lines for serial a programming of all ispLSI devices and two additional lines, which include the PCI9030 and the INTEL21150 devices. The LAN controller I82559 contains a special test interface, which is accessible via the molex connector TST. The BDM port of the main CPU MPC8245 is used for JTAG purposes as well as for the background debug mode.

The pin assignment of the ISP port is shown in the following table:

Pin:	Signal:	ispLSI mode:	JTAG mode:
1	TRST#		test reset
2	TDO		serial data out
3	VDD	3.3 Volts	3.3 Volts
4	TD12	serial data out	do not connect
5	TDI	serial data in	serial data in
6	ispEN	program enable	program enable
7	key		
8	MODE/TMS	mode control in	mode control in
9	GND	Ground	Ground
10	SCLK/TCLK	serial clock in	serial clock in

The daisy chain contains the following devices:

start of chain		tap of chain			end of chain
TDI	ispLSI2128	TD12	PCI9030	SB21150AC	TDO
---- ispLSI programming chain ----					
---------- complete JTAG chain ----------					

The pin assignment of the LAN test connector TST:

Pin:	Signal:
1	TEST
2	GND
3	TEXEC
4	TCK
5	TDI
6	TDI

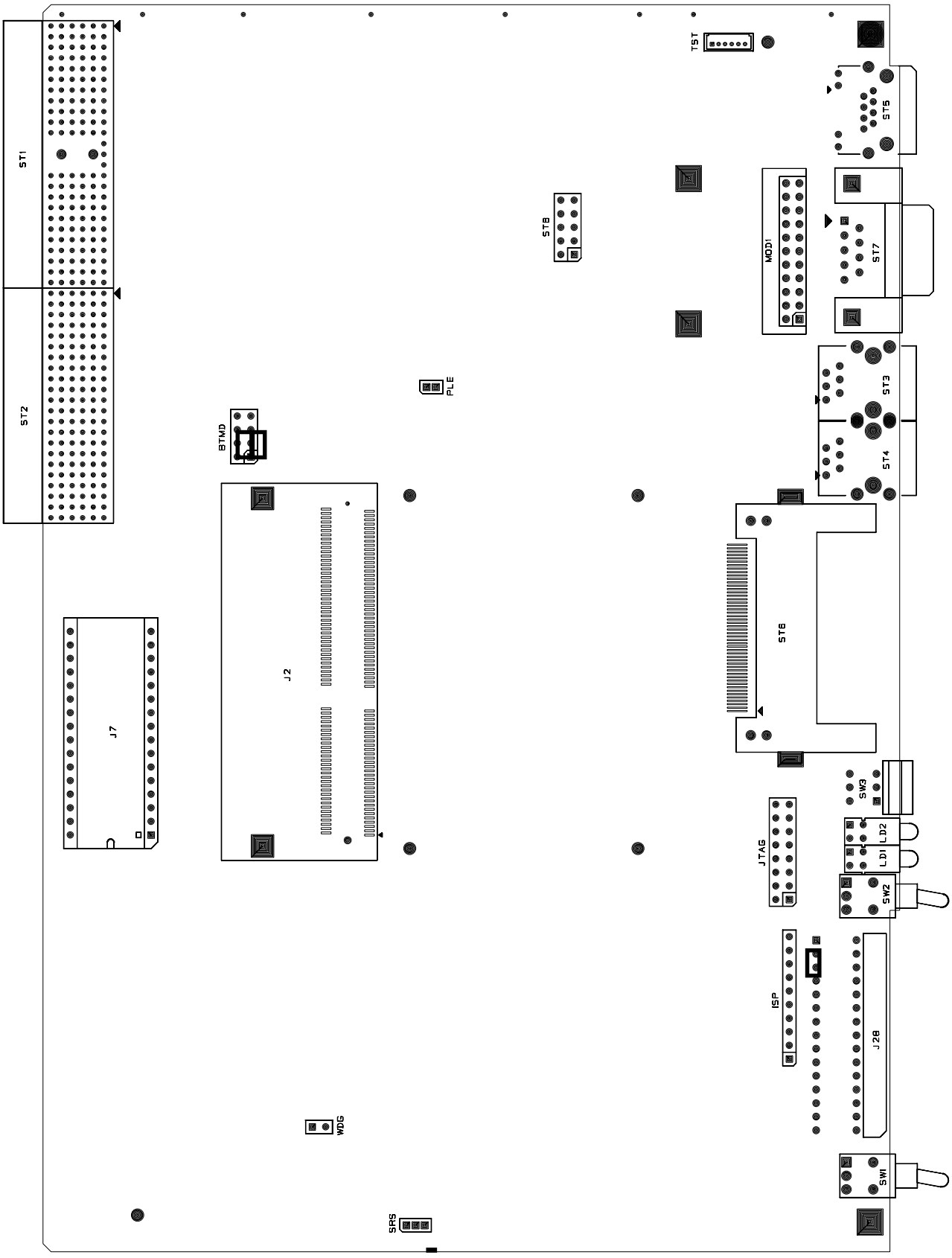
11. Summary of Jumper & Switches

Described function is valid, when jumper is set or link is intact !

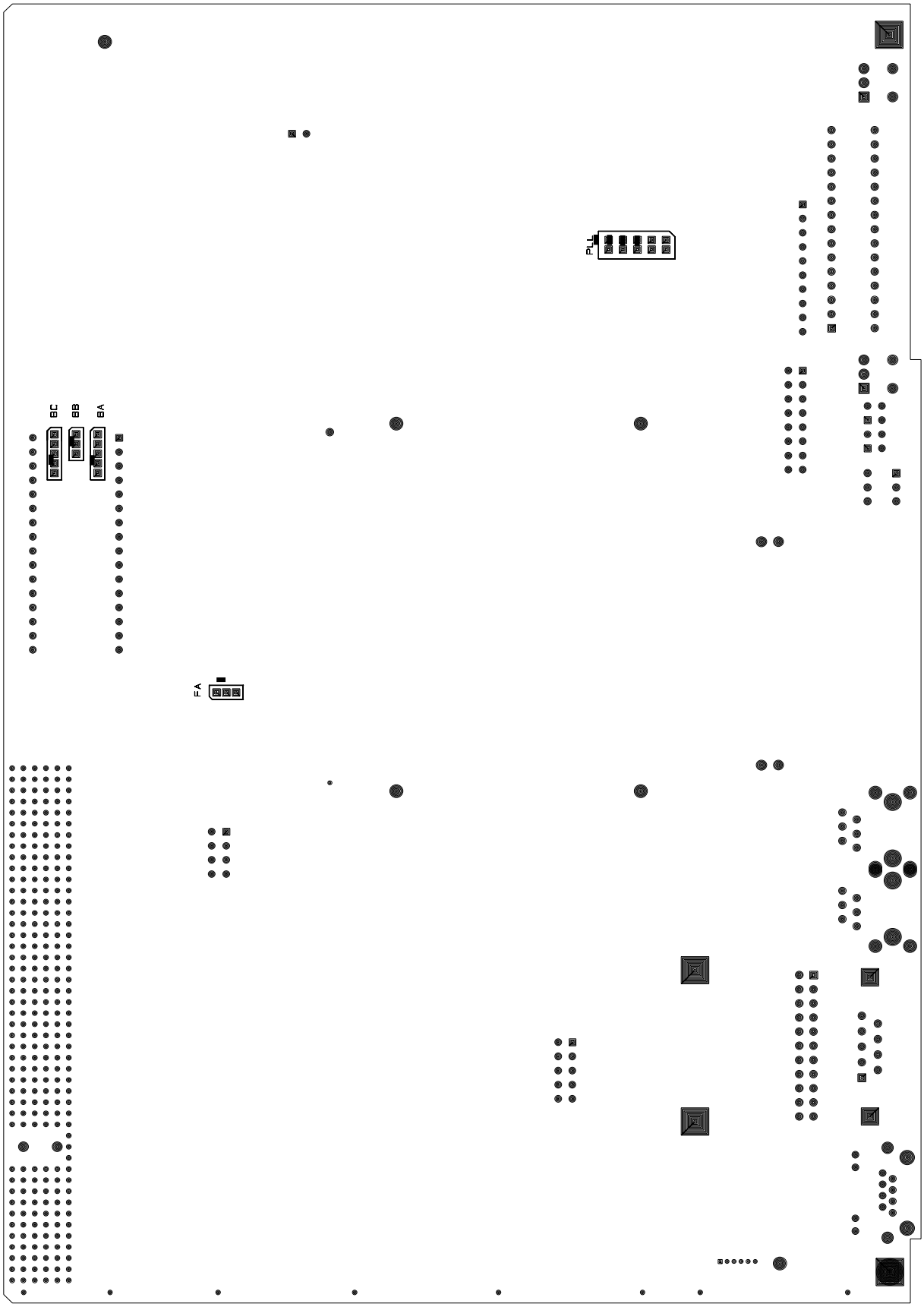
Size:	Name:	Default:	Position:	Function:
2x4	BTMD		1-2	CS2 connected to 8 bit flash
			7-8	CS3 connected to 64 bit socket
		#	3-5	CS1 connected to 64 bit socket
		#	4-6	CS0 connected to 8 bit flash
			3-4	CS0 connected to 64 bit flash
			5-6	CS1 connected to 8 bit socket
1x5	BA		1-2	socket pin 1 to Vdd
			2-3	socket pin 1 to A19
		#	4-5	socket pin 1 to A18
1x3	BB		1-2	socket pin 30 to Vdd
		#	2-3	socket pin 30 to A17
1x5	BC		1-2	socket pin 31 to Vdd
			2-3	socket pin 31 to A18
		#	4-5	socket pin 31 to RW
1x2	WDG		1-2	watchdog reset enabled
		#	---	watchdog reset disabled
1x10	ISP	#	9-10	8Bit socket is boot device
1x3	*FA*		*1-2*	*64 bit flash: ADV connected to CS*
		#	*2-3*	*64 bit flash: ADV connected to GND*
1x3	*SRS*		*1-2*	*SRAM Pin 30 to Vdd*
		#	*2-3*	*SRAM Pin 30 to LA19*
5x2	*PLL*	#	*1-2*	*see chapter 6.1.*
		#	*3-4*	*see chapter 6.1.*
		#	*5-6*	*see chapter 6.1.*
		#	*7-8*	*see chapter 6.1.*
			9-10	*see chapter 6.1.*

Note! Jumpers show in italic characters are factory set and should not be changed!

11.1 Jumper & Switches Component Side

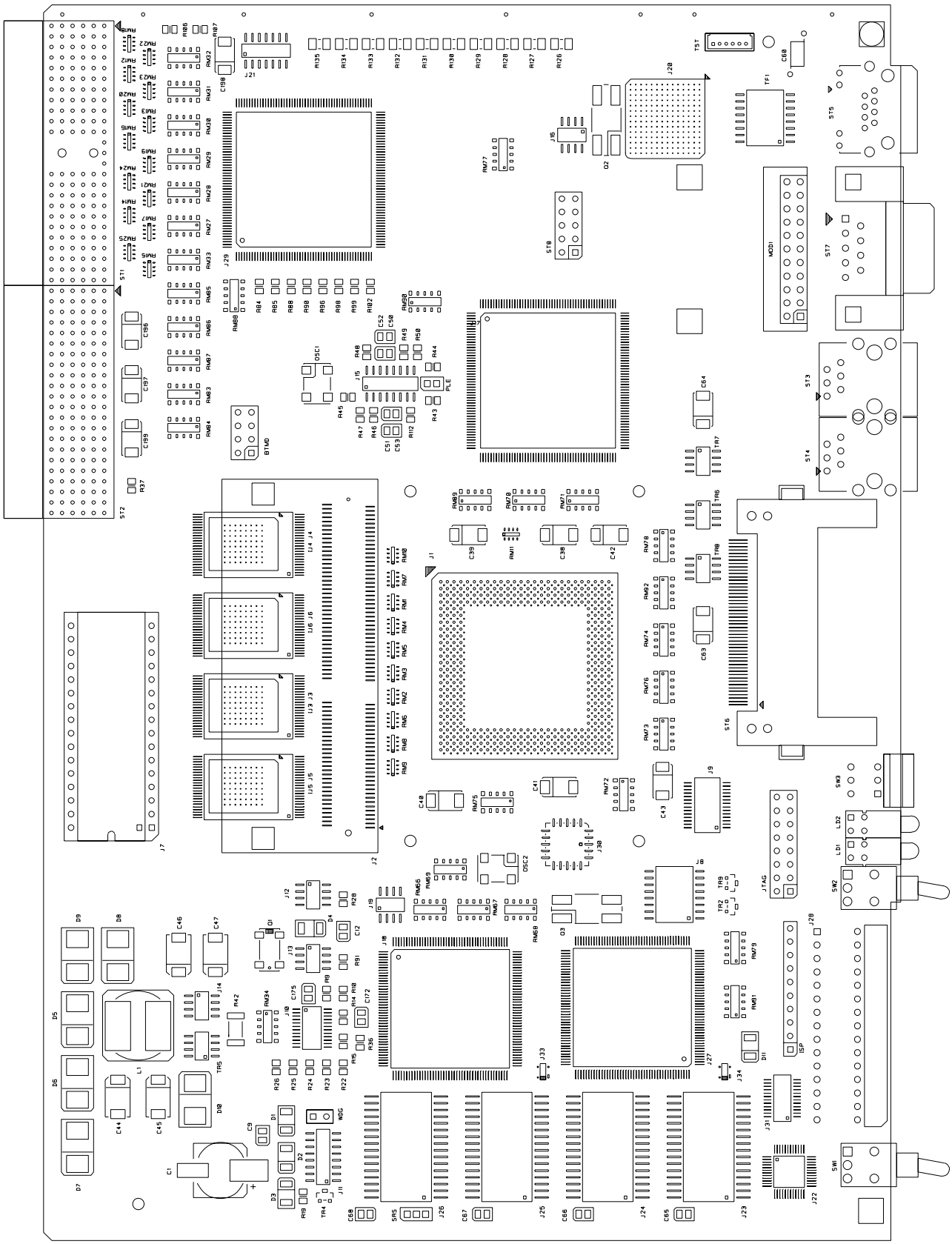


11.2 Jumper Solder Side

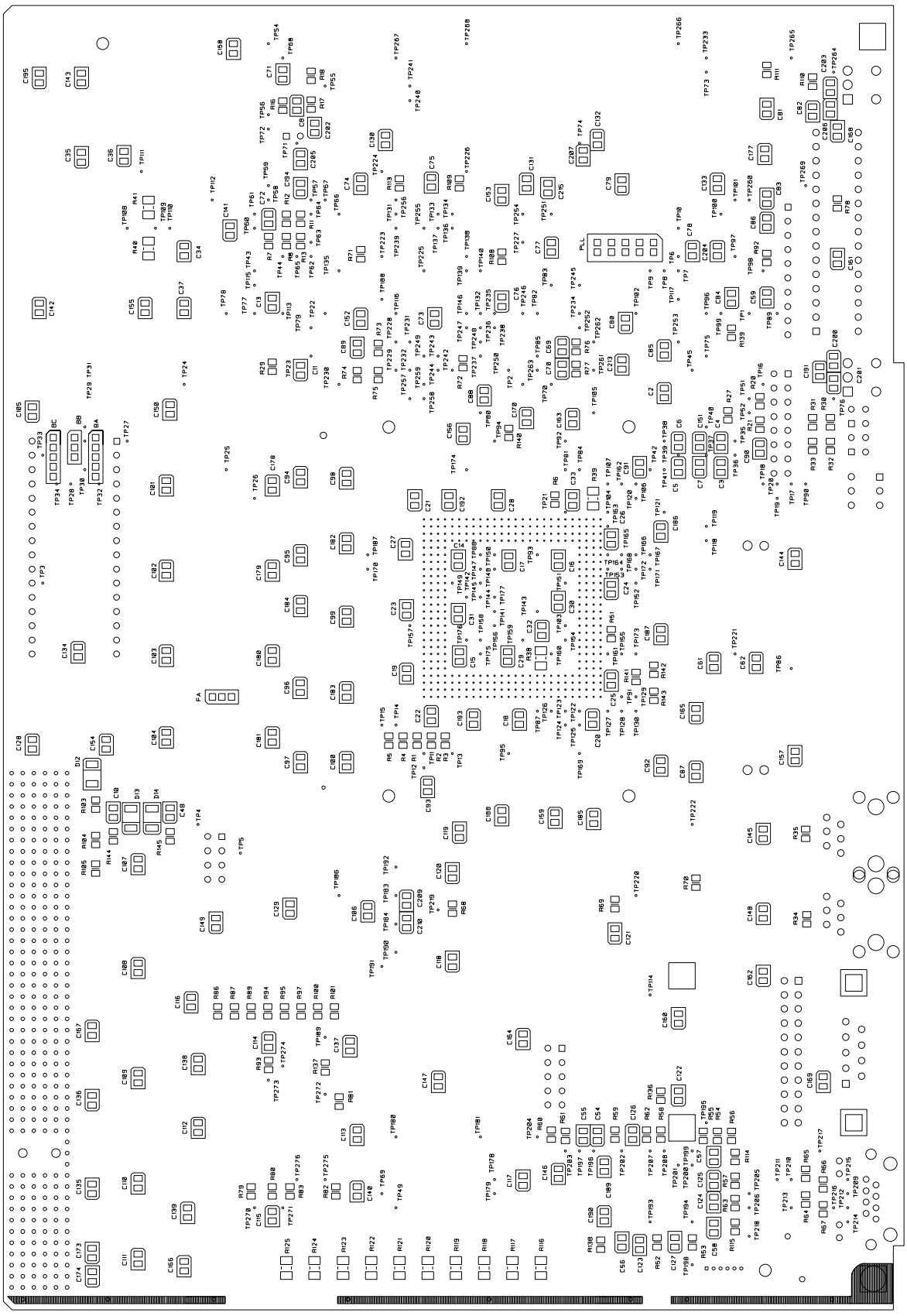


Appendices

Appendix A: Layout Component Side



Appendix B: Layout Solder Side



Appendix C: Schematics CPC45 (please contact *MicroSys*)